CSV 881: Low-Power Design   
Fall 2013

Homework 2 Problems

Assigned 24/10/13, due 25/10/13

**Problem 1:** A 32 bit bus operates at 1.0V and 2GHz clock rate. Each bit wire, driven by a CMOS buffer, has a total capacitance of 2pF. Each wire has a toggling probability of 0.75 per clock cycle. What is the total dynamic power dissipation of the bus drivers? Will the inversion encoding scheme reduce the power consumption?

**Problem 2:** A clock driver has a total output capacitance of 50pF. The supply voltage is 0.9V and the clock frequency is 2GHz. Calculate the power consumption of the clock signal.

**Problem 3:** Prove that a CMOS gate consumes no short-circuit power when VDD ≤ Vtn + |Vtp|, i.e., supply voltage is below the sum of the threshold voltage magnitudes for the n and p channel MOSFETs.

**Problem 4:** Using the Elmore delay formula, show that the delay of a long interconnect of length s is proportional to s2. Suppose, to reduce the delay of the interconnect we split it into two sections of equal length by inserting a buffer of delay d at the midpoint. Show that d must be less than half the delay of the original interconnect in order to achieve a delay reduction by this technique.