**VLSI Design & Test Seminar (ELEC7950-001 Spring 2016), Broun 235, Feb 17, 4PM**

**Illinois Scan Architecture:**

**Reduces Semiconductor Chip Test Cost**

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Test cost is a large fraction of total manufacturing cost of Semiconductor chips. Many ideas exist for reducing test costs. The ideas include Built-In Self-Test (BIST), novel Automatic Test Pattern Generation (ATPG) algorithms that reduce the number of test vectors, parallel scan to reduce scan load time and output data compression. All these ideas will be covered in this talk with pros and cons of each idea. In addition a novel Design for Test (DFT) scan architecture, now known as Illinois Scan Architecture will be introduced. Illinois Scan simultaneously lowers the hardware cost of Automatic Test Equipment (ATE) and operational cost of ATE, with an increase in test throughput. Some real chip examples from industry using Illinois Scan will be presented. It is shown that Illinois Scan can reduce test time and test data volume by a factor of 400 or more. Illinois Scan is now part of test tools from 3 of the 4 test cad companies.

**Janak H. Patel** is a Donald Biggar Willett Professor Emeritus of Engineering, and Research Professor of Coordinated Science Lab and Department of Electrical and Computer Engineering. He was founder of a Test CAD company, Sunrise Test Systems, which had the fastest commercial sequential ATPG and Fault Simulator. Sunrise was eventually acquired by Synopsis. He received a Bachelor of Science degree in Physics from Gujarat University, India and Bachelor of Technology in Electrical Engineering from the Indian Institute of Technology, Madras, India, and Master of Science and Ph.D. in Electrical Engineering from Stanford University. He is a Fellow of [ACM](http://fellows.acm.org/fellow_citation.cfm?id=1595982&srt=alpha&alpha=P) and [IEEE](http://www.ieee.org/web/membership/fellows/index.html) and a recipient of the 1998 [IEEE Emanuel R. Piore Award](http://www.ieee.org/portal/pages/about/awards/sums/piore.html) *for contributions to test generation and computer architecture*.

*Professor Patel will also give a colloquium talk, “Can we save Energy if we allow Errors in Computing?” in the ECE Department Broun 238 on February 18, 2016, at 3:30PM.*