Design a 32-bit ALU with sleep mode for 22 nm technology

**Abstract:**

 This project is meant to design a 32-bit ALU with a sleep mode for 22 nm technology in order to reduce power consumption when the ALU is not being utilized. This is generally done using a sleep transistor network. A sleep transistor network disconnects either VDD or GND from the circuit creating a virtual VDD or virtual GND where the value at the virtual VDD is close to GND and the value at virtual GND is close to VDD. This causes current not to flow and thus reducing the amount of power used by the ALU.

1. **Introduction**

In ASIC’s it is useful to be able to turn off or put to sleep components that are not currently being used as they still use power even when they are not being used. This is useful in power reduction usage which is good for mobile devices such as cell phones, handheld gaming, and tablets. When the device is not being used, which is most of the time, the device is still using power by means of leakage power. By adding a sleep mode to the device, we can reduce the power consumption by reducing leakage power. The most effective way to have a sleep mode is by power gating. Power gating is a method of disconnecting current from the logic block in order to disable current from being used through the block.

1. **Power gating design decisions**

In power gating, there are two techniques to gate a device. One is to use a pMOS header transistor gate, in which the device’s connection to VDD is disconnected and a “virtual VDD” is established where its value is very close to logic “0.” This reduces power consumption by not allowing the switching circuits in the ALU to actually turn on any transistors and thus, not use any power. The advantage to using a header gate is that pMOS transistors are less leaky than nMOS type but the disadvantages to a header gate is that pMOS transistors require more space than nMOS transistors because of their lower drive current. 

**Figure 1: Header and footer switch blocks for power gating[1]**

The other gating technique is using an nMOS footer transistor gate. This technique disconnects the GND and creates a “virtual GND” in which its value is very close to VDD and thus less than $|V\_{th}|$ so that the transistors never change state. The advantage to using nMOS transistors is that they don’t require as much space as pMOS transistors with the same drive current but they are more susceptible to ground noise and leak more than pMOS transistors. Also with a footer network, when the circuit is switched on from an off state, the current flow from the circuit can cause issues with ground bounce which can cause problems with in other circuits in which they may not function correctly.

For our design, we will use a footer transistor as the circuit will actually need a transistor network and not just a single transistor and as such, the network will require less room than the header transistor network.

For the design of the ALU, it has two functions, add and subtract with two 32-bit inputs and one 32-bit output.



**Figure 2: ALU design**

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**Figure 3: ALU with Sleep transistor**

1. **Power gate design[2]**

In designing the transistor network for the sleep mode we need a transistor network that will produce a high resistance when the gate is off so that the virtual GND is as close to VDD as possible while having a low on resistance so that when the transistor is activated, the voltage drop from “virtual GND” to GND is as low as possible. These requirements are very difficult to satisfy, as a transistor with a small on resistance requires a wider area transistor but with a wider transistor, the leakage is greater also.

In order to figure out the size of the transistor network, we need to figure out the delay of a single gate without the sleep transistor. This can be expresses as

$$τ\_{d}=\frac{C\_{L}V\_{dd}}{\left(V\_{dd}-V\_{tL}\right)^{α}}$$

where $C\_{L}$ is the load capacitance at the output, $V\_{tL}$ is the LVT = 350mV, Vdd = 1.0 V, $α$ can be taken as 1 for the technology.

 If a sleep transistor is added with a high Vt, the delay is calculated as

$$τ\_{d}^{Sleep}=\frac{C\_{L}V\_{DD}}{\left(V\_{DD}-V\_{x}-V\_{tL}\right)^{α}}$$

Where Vx is the voltage drop across the sleep transistor when active.

If we allow for a 5% overhead for the delay design, we get

$$\frac{τ\_{d}}{τ\_{d}^{Sleep}}=95\%$$

Solving the equation for $α=1$, we get

$$0.5\left(V\_{DD}-V\_{tL}\right)=V\_{x}$$

1. **Experimental data**

I was never able to get the software on the computers in the lab to work correctly and thus was unable to simulate my design. I was able to use Leonardo Spectrum to generate the Verilog netlist then import that into Design Architect-IC and from there the rest would not work.

The design would have had the ALU with the footer transistor network used. Testing would have been done using test vectors to measure the current with it always on, always off, switching half way in between, and also switching on every other input vector in order to measure worst case timing problems and how often the circuit could be switched on and off and still use the least amount of power. It would have been an attempt to find at what period the sleep mode could turn off and on at in order that its energy efficiency would equal the circuit that didn’t have the sleep mode.

1. **Conclusion**

While there are many techniques to reduce leakage power, one of the best is a sleep mode through power gating. Because of the failure on my part to get the circuit working properly and be able to simulate the design and do a power analysis, I am unable to come up with a clear conclusion as to how much power savings this design would have, but upon research in this area, I was able to find where people had been able to achieve up to 99% energy savings using A sleep mode with power gating.

1. **References**
2. David Chinnery, Kurt Keutzer, "Closing the Power Gap Between ASIC & Custom, Tools and Techniques for Low-Power Design", chapter 10, authored by Jerry Frenkil, co-author Srini Venkatraman, Springer 2007.

[2] Anis, M., Shawki, A., Mahmoud ,M., Elmasry, M., “ Dynamic And Leakage Power Reduction In MTCMOS Circuits Using An Automated Efficient Gate Clustering Technique”, Proc. of the 39th conference on Design Automation, June 2002, pp. 480-485