**Project 6 Final Report**

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**What did you learn from this project?**

Through taking the Computer Architecture this semester, I learned how to design and implement a CPU. Before taking on this project, I had no basic knowledge of the VHDL language, the project helped me to become familiar with the language and allow me to appreciate the beauty of this language. I worked on the tools ModelSim. I now understand the different steps involved in designing a single-cycle datapath.

**What would you do differently next time?**

If I were to do it all over again, I will focus on the part of design of data path and control. It became more and more obvious to me during the time I was working on the VHDL trying to implement the control and data path that a well-thought, careful-designed data path and control will make the implementation so much easier. I would work to make our design simpler, because me and my classmate ran into a lot complexity due to our complex design. I would also have started working with the Altera Quartus tools as soon as possible, so that we could resolve the errors created while running the code on the board.

**What is your advice to someone who is going to work on a similar project?**

I strongly advise those future students to work on with the first three part with great care. The upside of doing it is that you won’t be running into troubles such as the whole data path and control doesn’t not work as a whole even though each single component operates as expected. For debugging, one needs to thoroughly check each component in the datapath one by one which is time consuming, so verifying of the datapath after designing the control unit makes it simpler. Ask the teaching assistant for any help regarding the project.