TO: Prof. V. Agrawal, Yun Wang
FROM: Alan Hoffman
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SUBJECT: Project Part 6: Final Report

**What did you learn from this project?**

During the course of this project I learned a lot about the basics of CPU design. Since most of the design decisions were left up to the student, I had a lot of choices to make at each step. First, I learned how to develop an ISA for a fixed size microcontroller. Then, I learned how to design a model of a datapath using different hardware units like ALUs, MUXs and logic gates. Once this design was completed, this model was implemented in VHDL and simulated to verify correctness. Finally, the VHDL implementation was integrated with memory and checked once again. These final steps taught me a lot about the value of hardware description languages and about how easy they make it to design and simulate a processor.

**What would you do differently next time?**

If I was to do this project again, I might try to do a pipelined datapath rather than a single-cycle datapath. I chose to do a single-cycle datapath because it was the simplest of the possible designs. Now that I have a better understanding of how everything works, I might try to do a pipelined datapath to make my overall design more efficient.

**What is your advice to someone who is going to work on a similar project?**

My advice would be to read all of the requirements before starting the project. Understanding some of the later requirements will influence the design decisions you make in the early steps of the project. Using the examples in the class slides as a basis for your designs is also very helpful for many of the steps.