ELEC 6200 **Sowmya Seelam**

CPU DESIGN PROJECT REPORT **Abhishek kulkarni**

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What did you learn from this project?

Designing and implementing a CPU has been a great learning experience in this course, starting with project we had basic knowledge of the VHDL language, but the project helped us to become aware with the beauty of this language. We worked on the tools like ModelSim, Quartus and used Altera FPGA Boards starting from part 3 of the project although the FPGA board was used only for implementing our CPU design in part 5. We now understand the different steps involved in designing a multi-cycle datapath. In the final step of the project, we learned how to simulate our processor on the Altera FPGA board provided in the lab and how to use the *In-System Memory* tools to run our test program straight from the Quartus software.

What would you do differently next time?

We would work to make our design simpler, because we ran into a lot complexities due to our complex design. We would also started working with the Altera Quartus tools as soon as possible, so that we could resolve the errors created while running the code on the board. For instance, we faced problems while executing the branch and jump instructions for executing loops. Individually the two instructions were working fine, and there were no errors in the ModelSim simulations, but we could not make them work in the Quartus II tool. The problem was related to the updating of the program counter. Also we initially used the clock with 27MHz (Pin_D13) but it failed to change the state of the control unit. So we used the clock of 50MHz to implement it in our design. Also next time we would be aggressive to take up the challenge of implementing the Pipelined Datapath incorporating the Hazard Detection and Forwarding unit. We got some problem with the arithmetic overflow i.e. our ALU did not report the correct value for very large product terms. We would definitely like to implement this functionality in our VHDL model in future.

What is your advice to someone who is going to work on a similar project?

We strongly advise you to work on each part regularly. At the End, for debugging, one needs to thoroughly check each component in the datapath one by one which is time consuming, so verifying of the datapath after designing the control unit makes it simpler. Also don't compile your project directly from the H drive, save it in C drive for the compilation as it saves plenty of execution time. Ask, the T.A for any help regarding the project, she is always ready to help you.