SINDHU GUNASEKAR

SAKETH ANUMA REDDY

ELEC 6200 – CPU design project - Report 5

1. This project helped us learn VHDL and get familiarized to the tools Modelsim and Quartus II. Most importantly, it helped us understand completely the organization of the RISC.
2. In case we redo the project, we will try to implement it with a pipeline datapath.
3. For those who are going to do the project in the future, we would recommend to start at least a month before the final demo. It could help to verify the simulation of the control signals and each and every component in the datapath. The startup could be time-consuming, especially if you haven’t worked on VHDL before. But the project really gets exciting toward the end.