**ELEC 5200 Report**

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**What did you learn from this project?**

Modelsim simulations are not necessary to be synthesized due to real time implementation of our design; this was a quintessential part of our learning through the course of this project. Another key aspect was not to include combinational logics within the process statement; which eventually resulted in numerous unwanted latching within our design. Checking of memory elements was performed due to which we had to re- design few elements in our project.

Before kicking off with the project we had an initial layout in order to design and synthesize the CPU. This project gave us in-depth details on synchronous and asynchronous elements and how they get acquainted together.

**What would you do differently next time?**

Given another chance on a different day and time we would try to implement either single cycle data path or Pipelining Architecture. With single cycle data path we would like to implement new instructions, whereas pipelining would be difficult as we would have to take care of data hazards but if implemented in legitimate ways it could turn out to be appreciable.

**What is your advice to someone who is going to work on a similar project?**

Start early and stay within time limits. Always test each and every component within the board after simulating it. Design should be simple, avoid complex structures and test the design thoroughly during simulation because when it is implemented on the board, things will seem oblivious and hard to debug.