Final report on Multicycle Datapath with Finite State Machine as Control unit

*Insight of the Project:*

Implementing a CPU with Multicycle as the datapath and a Finite State machine as the Control unit has not only helped me discern the hierarchical architecture of a computer but also the functionality of individual hardware components used. I could also interpret the functioning of various instructions that are categorized into R, I and J type. The experience of simulating the project on Modelsim and Quartus-II kit has helped me understand the interfacing between the software and the hardware components of the project. Overall, I feel that this project delivers the required intuition for an individual with an overview on Computer Architecture.

*Future enhancement of the project:*

I would implement the datapath using pipelining where each instruction on an average, is executed in a single cycle. But, we need to overcome the hazards that aren’t seen in multicycle datapath. Thus, using pipelining, though is an efficient technique requires stringent measurements to eliminate the hazards, which further helps me learn the handling of hazards. I would also like to implement a microcoded control unit, which is flexible than the FSM. Software-like changes to the instruction set and emulation of completely different instruction sets are the major advantages in using this Control Unit.

*Suggestions to Students working on this project:*

It is recommended to understand the functioning of the project before practically implementing, as this would give a good insight over the project. While working on the project, I would suggest the students to verify the functioning of each and every component used in the datapath and also the control signals for every instruction used, as debugging at this stage is effortless, on the other hand the same debugging becomes very complicated and time consuming while executing the project on the kit. There will be a lot of hurdles while running the code on the FPGA kit, so it is important to start the final part as early as possible.