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CPU Design Project Part V:

Report

At the beginning of the semester, having heard of VHDL just in Digital Logic, it was first difficult for me to understand what the project was about at first sight. The first thing that came in my mind was dropping the class, but after taking a good look at part one of the project, I found out that it was feasible using the courses material and the help of the teacher, the teaching assistant and my classmates. I had to familiarize myself with RISC design principles; I had to understand and design an instruction set architecture while respecting the design principle, I had to design my datapath from scratches while thinking about each of my instructions. One of the biggest things I have learned was coding, simulating in VHDL/Verilog and using the FPGA board. The fact that I had to understand what the instructions, and components of the datapath were used for helped me understood how I was supposed to implement each components in Modelsim. From the beginning of the project, designing the instruction set architecture, to the final part, designing and implementing the circuit on the FPGA, were all new and good learning experiences.

Even though I have learned a lot doesn’t mean I didn’t or still do not have many issues. I didn’t really understood what was the outcome of the project as I was choosing the needed instructions. While implementing them in the datapath or the control unit part, I was having difficulties, resulting in the change of some instructions and the datapath. What I will do differently is try my best to really understand what the expected outcome is at the beginning of project, understand why I am doing every single thing while moving forward with the project. I should get help as soon as needed instead of wasting too much time on a single problem and delay the completion of a part. Another issue delaying the completion of the project was my lack of experience with VHDL/verilog so I think I should have learned more about it before starting the project or at least part three.

Everybody supposed to work on a similar project, should first read thoroughly the project and understand as much as possible what the outcome of the project is. Everybody should get a partner unless you really understand what RISC CPU design is about and you are very familiar with VHDL. In case you have little or no knowledge of what VHDL is, you have to get familiar with it through books, papers or sit in ELEC 4200 if permitted before starting the project, particularly part three. At the end of the project, after implementing the circuit on the FPGA, there was no signal received on the DE2 board. I assumed my program counter was not working, so I connected my PC output to the switches on the board, still no result. It is a good idea to verify each component and make sure everything is right before connecting them together.