**CPU Design Project**

**Part 5**

**What did you learn from this project?**

I learned how to design a CPU using VHDL and implement it on a DE2 FPGA board from Altera using Quartus II software. I learned the various steps needed to design a CPU: choosing an ISA, designing a datapath, verifying that datapath with a simulator such as ModelSim, design of a control unit, creating a top level design to join datapath with memory and control unit, and hardware implementation.

**What would you do differently next time?**

I would probably experiment more with different datapaths. Although I am content with my design, I would have liked to try optimizing it more if possible by trying other datapaths and comparing the performance. Another thing I would do differently is manage my time better. Dividing the work of each section between a few days would have allowed for more time to deal with unexpected problems. Instead, I ended up rushing to get done for most of the later parts of the project. I also would have tried hardware implementation earlier than one day before the demo. Although my CPU ran through the simulation without error, there were a few problems with the hardware implementation that took some time to correct or at least find a temporary solution.

**What is your advice to someone who is going to work on a similar project?**

I would strongly suggest time management. The earlier you start each part of the project, the more time you will have to find and correct problems and optimize your design. I would also suggest hardware implementation as soon as possible. There are some problems that will be hard if not impossible to find just by simulation. Although I am pleased with my design, I know it would be better if I had managed my time better during the development.