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**What did you learn from this project?**

We learned how to design individual components of a processor that we have been learning about in class. More importantly, we learned how each of these components fit and work together. Modeling these components in VHDL was very beneficial, as well. We were able to understand the complete process of designing a process, from the instructions and register definitions to the final testing on hardware. We learned how to create a runtime editable memory module with the Altera software, which helped in the testing process. Also, we were able to physically see the differences in using a single-cycle processor versus a multi-cycle processor. Ultimately, we were able to apply the theory we learned in lectures to actual hardware, which was the best learning experience we could have.

**What would you do differently next time?**

We realized the deficiencies of a single-cycle datapath during our development of our processor and would most likely attempt to implement a multi-cycle processor instead. Also, we would think further ahead in the design process in order to not have to keep changing up our instruction and register formatting. This was an issue we had to deal with as we moved into another part of the project and we realized what we currently had was not feasible or as efficient as it could be. Overall, our process and approach went very well and wouldn’t change much else.

**What is your advice to someone who is going to work on a similar project?**

We had to make several changes to our instructions and register formats during several stages of the process. This was due to us not understanding the requirements of each part and component from the beginning. Our advice would be to read through each part carefully and try to fully visualize what the requirements will be for each component before defining your instructions and registers.