FIRST INTERNATIONAL WORKSHOP ON VLSI DESIGN

December 26-28, 1985

Sponsored by
Computer Society of India
IEEE India Council

Program Coordinators

Vishwani Agrawal
AT&T Bell Laboratories
Murray Hill, NJ 07974
USA

H. N. Mahabala
Indian Institute of Technology
Madras 600 036
INDIA
FIRST INTERNATIONAL WORKSHOP ON VLSI DESIGN
Madras, India, December 26-28, 1985

Program

(Papers included in this digest are marked with *)

December 26, 1985

09:00 AM  Introduction  Prof. H. N. Mahabala, IIT, Madras
09:15 AM  Inauguration Address  Dr. O. P. Mehra
            President
            Computer Society of India

10:00 AM  Break

10:30 AM  Session 1  S. Hulsoor, Chairman
            Digital Equipment Corporation
            VLSI Design
            Jacob Abraham, University of Illinois, Urbana, IL
            VLSI Testing*
            V. D. Agrawal, AT&T Bell Labs, Murray Hill, NJ
            VLSI Technology
            A. B. Bhattacharya, IIT, Delhi

12:30 PM  Lunch

02:00 PM  Session 2  C. Pandurangan, Chairman
            IIT, Madras
            VLSI Architectures and Algorithms*
            V. K. Prasanna Kumar, University of Southern California
            Time-Model Analysis of PA³ Arrays
            N. Venkateswaran and K. M. M. Prabhu
            IIT, Madras
            A Systolic FIFO*
            Z. Ali and A. Al-Khallili
            Concordia University, Montreal, Canada

03:30 PM  Break

04:00 PM  Session 3  A. Prabhakar, Chairman
            ITI, Bangalore
            Routing Algorithms
Generalized 2-Layer Channel Router  
V. Jagadeesh and K. S. Raghunathan, ITI

A Router for CMOS Single Metal SCL Gate Array  
V. S. Raghunath and A. Kumar  
SCL

On Single Row Routing  
S. Arunkumar, IIT, Bombay

05:30 PM  Dinner Break

08:00 PM  Session 4  
VLSI in India  
(Panel Discussion)  
H. N. Mahabala, Chairman  
IIT, Madras

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08:30 AM  Session 5  
Design For Testability  
D. K. Pradhan, Chairman  
University of Massachusetts

Built-In Self Test in VLSI/WSI*  
V. K. Agarwal, McGill University

Universal Testability of nMOS RMC Networks for Detecting Physical Failures*  
B. Gupta, ISI, Calcutta  
B. B. Bhattacharya, University of Nebraska  
G. S. Basu, Ministry of Communication

On the Effect of Physical Failures in CMOS Logic Networks  
M. S. Babu and D. K. Sultania  
SCL

Effect of Activity Variation on VLSI Reliability*  
R. K. Iyer, University of Illinois

10:30 AM  Break

11:00 AM  Session 6  
Simulation  
Jacob Abraham, Chairman  
University of Illinois

Mixed-Mode Simulation of MOS Integrated Circuits*  
P. Subramaniam, AT&T Bell Labs

MOSIMR: A Mixed-Mode Simulator using Signal Propagation to Exploit Latency  
S. Banerjee and R. Raghuram, IIT, Kanpur

Hardware Accelerators*  
P. Agrawal, AT&T Bell Labs
12:30 PM  Lunch

02:00 PM  Session 7
PLAs in VLSI  V. K. Agrawal, Chairman
McGill University

VLSI Topological Optimization Applied to PLA Design:
A Survey*
P.Dash,SCL

Design and Simulation of PLA
M. M. Hasan, IIT, Kanpur

On the Design of Testable PLAs*
S. M. Reddy, University of Iowa

03:30 PM  Break

04:00 PM  Session 8
Test Generation  V. D. Agrawal, Chairman
AT&T Bell Labs

FLATPAG Functional Level Automatic Test Pattern Generation*
for VLSI - An Integrated Approach
P. Das Gupta, M. Gerner, and W. Feiten
Siemens AG, Munich

What Heuristics are Best for Podem?*
J. H. Patel, University of Illinois

Function-Based Test Generation for Microprocessors
P. S. Ramaiah and V. R. K. Murthy, Andhra University

05:30 PM  Evening Program and Dinner

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08:30 AM  Session 9
Silicon Compilers  Dr. Zarabi, Chairman
SCL

A VLSI Chip Generator using Dataflow Methodology*
V. P. Srinivas and A. M. Despain
University of California, Berkeley

Storage/Logic Arrays: Can they Rival Handcrafted
VLSI Solutions?*
H. Ravindra, S. S. Patil, and Bill Knapp
Cirrus Logic, Inc.

Design and Implementation of a Translator from ICL to CIF
A Component in Silicon Compiler
S. Prithviraj, R. Sankaranarayanan, T. S. Krishna Kumar,
H. N. Mahabala, IIT, Madras
10:00 AM  Break

10:30 AM  Session 10  Physical Design  Prathima Agrawal, Chairman  AT&T Bell Labs

A Symbolic VLSI Layout Design System  
G. T. Chari, ITI

IV: An Interconnect Verification Program for Verifying VLSI Layout*  
K. L. Kodandapani, DEC

General Design Rule Checker for IC Layout  
K. S. Raghunathan and A. Prabhakar  
ITI

Test Pattern for Parameter Extraction and Process Control  
D. A. Mohan, R. Nagendran, and R. Ganesan  
BEL

Special Session  Dr. L. S. Srinath, Chairman  
Director, IIT, Madras

Welcome  S. Satyanarayanan, CSI Madras Chapter

Workshop Summary  Dr. V. D. Agrawal

Workshop Conclusions  Dr. H. N. Mahabala

Valedictory Address  Microelectronics - Indian Perspective  
Dr. M. S. Sanjeevi Rao

Chairman’s Remarks  Dr. L. S. Srinath

Vote of Thanks  M. V. Chauhan, IEEE India Council

1:00 PM  Lunch

2:00 PM  Discussion with IIT Students  Dr. V. D. Agrawal, Chairman

Topic: Problems of Engineering Education in India