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A Defect Tolerant and Performance Tunable Gate Architecture for End-of-Roadmap CMOS

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Abstract

In addition to high defect rates, end-of-roadmap CMOS at sub-10 nm gate lengths is also expected to display significant random variability in individual device performance. This will lead to unique and varied slow paths (statistical performance outliers) in individual ICs, severely limiting achievable clock rates. While it is widely accepted that to ensure viable manufacturing yield and reliable field operation, future circuits will need to be equipped with significant defect-tolerance capabilities, it is less commonly recognized that continued performance gains from scaling in the face of extreme parameter variations will also require a post manufacture performance tuning capability capable of speeding up the statistical slow paths on individual ICs that limit clock rates. In this paper, we show how a recently proposed defect-tolerant CMOS logic gate architecture can efficiently achieve both these goals. Our basic design exploits the inherent functional redundancy in static CMOS for defect tolerance; the CMOS logic gate is reconfigured to a pseudo-NMOS-like gate in the presence of a defect by using an appropriately sized single pull up or pull down transistor to replace the defective pull-up or pull down network. Thus the resulting defect-tolerant gate architecture can tolerate defects in either the pull-up or pull-down network and incurs only a modest area overhead. Multiple defects across the logic gates in a large CMOS design can also be tolerated. Importantly, these redundant pull up or pull down transistors can also be strategically turned on for performance tuning, speeding up a slow critical transition through a gate at the possible expense of a small slow down in the opposite transition. Results evaluating the effectiveness of the new defect tolerance and performance tuning technique are presented.

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