Qualifying Exam Information: Computer Organization and Architecture

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Note: This study guide contains a few sample questions that provide an indication of the skills that we expect you to demonstrate in the topic areas of computer organization and architecture. See the end of the document for a list of these skills, topics covered by this qualifying examination and suggested readings. In general, you should expect questions that address the listed skills in any of the listed topic areas. These topics are those covered by typical junior/senior/first-year-graduate courses on computer organization and architecture. A specific topic may or may not be covered by the undergraduate/graduate courses you took or by our COMP3350, COMP4300, or COMP7300. Nevertheless, you are still responsible for knowing this topic. To become familiar with these topics, you are encouraged to read relevant chapters from the suggested book or any other books on computer organization and architecture.

Sample Questions

Question 1. True or False? Assembly language identifiers are by default case insensitive. (Answer: True)

Question 2. True or False? When a program’s source code is modified, the source code does not need to be assembled and linked again before it can be executed with the changes. (Answer: False)

Question 3. Write an instruction that subtract val3 from EAX
   A. sub val3, eax
   B. sub eax, val3
   C. subtract val3, eax
   D. subtract eax, val3
   (Answer: B)

Question 4. Which of the following is the implementation of AX = (-val2 + BX) - val4 in assembly language?
   A. mov ax, val2
      neg ax
      add ax, bx
      sub ax, val4
   B. mov ax, val3
      neg ax
      add ax, bx
      sub ax, val4
   C. mov ax, val2
      neg ax
      add ax, bx
      add ax, val4
   D. mov ax, val2

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add ax
add ax, bx
sub ax, val4

Answer: A

Question 5. Which of the following state is FALSE?
A. The LOOP instruction repeats a block of statements a specific number of times
B. JMP is a conditional transfer instruction
C. Assembly language programs use conditional instructions to implement high-level statements such as IF statements and loops
D. Each of the conditional statements involves a possible transfer of control (jump) to a different memory address

Answer: B

Question 6. True or False? Moore's Law states that the performance improvement to be gained from using some faster mode of execution is limited by the fraction of the time the faster mode can be used.

Answer: False

Question 7. True or False? The fundamental idea of instruction pipelining is to split the processing of a computer instruction into a series of independent steps, with storage at the end of each step.

Answer: True

Question 8. CPU execution time for a program depends on the following except
A. Process management
B. CPI
C. Instruction count
D. Clock cycle time

Answer: A

Question 9. Data hazard solutions include the following approaches except
A. Reordering
B. Forwarding
C. Stalling
D. Predict

Answer: D

Question 10. Given a four-stage scoreboard, what types of hazards must be detected during the read-operands stage?
A. structural hazard
B. WAW hazard
C. RAW hazard
D. No hazard

Answer: C
Skills
- Describe methods used to encode standard data types to be stored and manipulated at the machine level.
- Demonstrate the ability to program microprocessors in assembly language.
- Show how to make use of standard data structures (e.g., arrays) in computer memory and explain how these structures are accessed at the machine level.
- Learn the principles behind the design of modern computer systems
- Understand the design of instruction sets
- Learn pipelining techniques
- Understand issues in hierarchical memory system design
- Classify and describe parallel computer architectures

Topics
- Assembly language programming
- Conditionals and integer arithmetic
- Data representation
- Addressing and arithmetic
- Strings and arrays
- Principles of instruction set design
- Computer arithmetic
- Pipelining
- Memory hierarchy
- Autonomous I/O
- Quantitative characterizations of CPU
- Memory and I/O performance.

Textbooks

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