Analog Implementation of Pulse-Coupled Neural Networks

Yasuhiro Ota and Bogdan M. Wilamowski, *Senior Member, IEEE*

***Abstract*— This paper presents a compact architecture for analog CMOS hardware implementation of voltage-mode pulse-coupled neural networks (PCNN's). The hardware implementation methods shows inherent fault tolerance specialties and high speed, which is usually more than an order of magnitude over the software counterpart. A computational style described in this article mimics a biological neural network using pulse-stream signaling and analog summation and multiplication. Pulse-stream encoding technique uses pulse streams to carry information and control analog circuitry, while storing further analog information on the time axis. The main feature of the proposed neuron circuit is that the structure is compact, yet exhibiting all the basic properties of natural biological neurons. Functional and structural forms of neural and synaptic functions are presented along with simulation results. Finally, the proposed design is applied to image processing to demonstrate successful restoration of images and their features.**

***Index Terms*— Annihilation, CMOS, image processing, neuromorphic pulse delay lines, neuron coupling strength, refractory period, threshold point, VLSI.**

I. Introduction

The elementary computing units of the nervous system are neurons. A human brain apparently has 10^{12} cells with 10^{15} interconnections for processing information. In the vertebrate nervous system, communication between distant neurons is accomplished using encoded pulse streams [1], [2]. It was well into the 1930's before significant measurements of pulse-coded electrical activity in the brain had begun. Among those making such measurements in the 1930's was Schmitt [3], who devised a means of solving the equations proposed in theories of biological impulse propagation via vacuum tube circuits. In any event, the neuristor and its derivatives led to a large number of circuits being proposed for neural network realizations in mid 1960's through the mid 1970's. The main results to come out of this research activity in the pulse-stream hardware area were the development of a bipolar circuit that acted as an action-potential-like-pulse generator by Wilamowski, et al. [4], its companion circuit by Newcomb *et al.* [5],[6]. The idea of the neuristor is to abstract the five key axon properties of 1) threshold of excitation; 2) refractory period; 3) constant pulse-propagation velocity; 4) pulse-shaping action during its propagation through the neuristor line; and 5) annihilation of pulses in case of their collision.

Manuscript received January 28, 1997; revised January 3, 1999.

The authors are with the Department of Electrical Engineering, University of Wyoming, Laramie, WY 82071 USA.

Publisher Item Identifier S 1045-9227(99)03186-0.

The hardware implementation methods shows inherent fault tolerance specialties and high speed, which is usually more than an order of magnitude over the software counterpart. Pulse-stream encoding technique [7]–[22] uses pulse streams to carry information and control analog circuitry, while storing further analog information on the time axis. This approach lends itself naturally to continuous computation, as in the conceptually simple but theoretically rich feedback networks introduced by Hopfield [23].

Several pulse-coupled techniques are pointed out by Murray *et al.* [7]. They organized and summarized nicely on the advantages and disadvantages of 1) pulse amplitude modulation; 2) pulse width modulation; 3) pulse frequency modulation; and 4) pulse phase modulation techniques. The firing rate of action potentials in biological neurons is roughly proportional to change in the original graded potential, which is categorized as frequency modulation. Thus, the design presented in this paper follows the natural biological process and utilizes the frequency modulated neuron system. A chopping clock signal [8] is introduced, which is asynchronous to all neural firing and is logically high for exactly the correct fraction of time to allow the appropriate fraction T_{ij} of the normalized synaptic weights ($-1 \leq T_{ij} \leq 1$).

The postsynaptic weights are then obtained by AND-ing the chopping clock signal with the input (presynaptic) signal with a digital circuitry. In the article [9], capacitors are used to represent synaptic weights, and a self-timed communication scheme that multiplexes neural state information asynchronously is used with digital RTT/RTR handshake control data transmission lines. Another pulse duty cycle modulation technique described by Moon *et al.* [10] has no need for a clock to synchronize pulses or to adjust pulse width. This pulse duty cycle modulation technique is used on the output pulse stream of their neuron-type cell and is controlled by changing a voltage variable resistance in the neuron-type cell. A frequency modulated pulse-firing circuit with programmable synapse electronic circuits with floating-gate MOS transistor is introduced [11]. The threshold voltage of a floating-gate MOS transistor is adjustable in small steps via the application of programming pulses between the control gate and the substrate. Pulse-mode neural circuits based on a multiquantum well injection mode device (MQW-IMD) was proposed [12]. This circuit uses a simple discrete RC load, which switches periodically between a low conductance off state and high conductance state generating a pulse mode output, exhibiting its sigmoidal-type current-voltage characteristic and a threshold behavior. An adaptive neural processing node with on chip learning

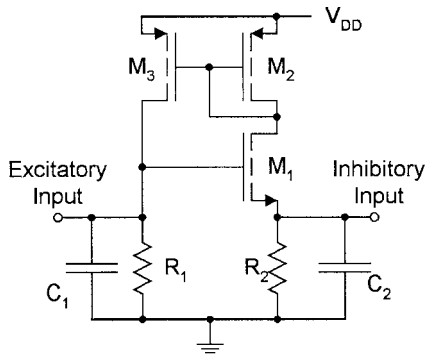


Fig. 1. Concept diagram of the pulse-coupled neuron cell.

using the unsupervised weight modification rule [13], [14] demonstrates the capability of producing linearly separable outputs that correspond to dominant features of the inputs. Statistical models of PCNN using digital circuitry are also proposed by other researchers [15], [16]. A statistical model of error (or noise) is developed to estimate relative accuracy associated with stochastic computing in terms of mean and variance in these designs. Padgett *et al.* [24] present overview of the use of PCNN in pattern recognition applications, and it is also covered in more detail in several articles [25]–[29].

II. CMOS Model of Pulse-Coupled Neuron

Inspired by biological models and the advantages of PCNN, a simple integrated circuit structure for a neuron with synaptic weight multiplication and summation is described in this section. The neuron circuit and its associated circuit's function like a biological neuron with synaptic junctions. The concept diagram of the neuron cell circuitry shown in Fig. 1 is an electronic analogy of a biological soma; i.e., it initiates reactions, with a given external stimulus, by generating a stream of electrical pulse waves. In this case, the external stimulus is current. The circuit structure is based on the current-driven simple neuron cells [16]–[18]. Synaptic weights in these current-mode neuron cells are controlled by current mirrors at the output of the neuron cell with proper W/L ratios.

The proposed voltage-mode neuron cell in Fig. 1 functions as follows. The circuit has two capacitors, C_1 and C_2. The stored charge on capacitor C_1 corresponds to the charge of sodium ions (Na^+) accumulated on the external side of the neuron membrane, and the charge stored on C_2 corresponds to the potassium ions (K^+) accumulated inside the neuron cell [18]. The potential due to sodium ions changes at a faster rate than the potential due to potassium ions. Therefore, the time constant of the C_1 circuit is made smaller than that of the C_2 circuit. In a steady state, all the MOS transistors (M_1–M_3) are cut off. As the potential on C_1 increases and exceeds the potential on C_2 by the threshold value of transistor M_1 at some point, then transistor M_1 change its state into active region of operation and further activates transistors M_2 and M_3 which form a current mirror. This positive feedback through transistors M_1, M_2, and M_3 is quickly terminated once capacitor C_2 is fully charged, and all the transistors become turned off. During the recovery process, known as

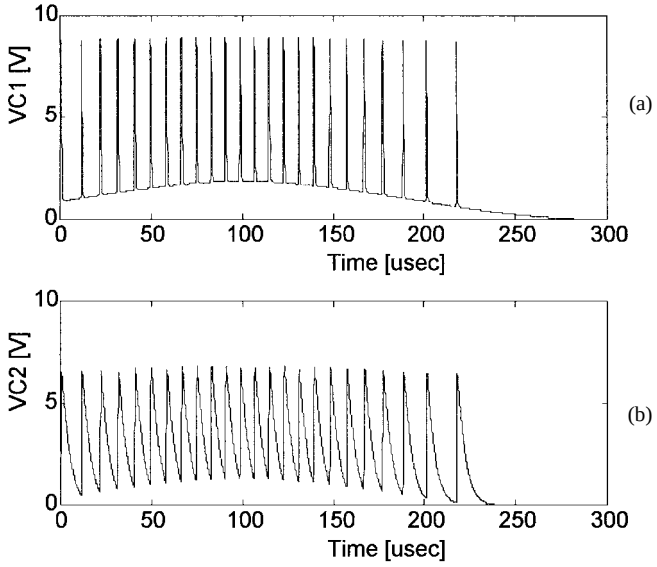


Fig. 2. SPICE simulated transient response of the circuit of Fig. 1 excited with a shifted sinusoidal input. The top graph shows the response on capacitor C_1, and the bottom graph shows the response on C_2. Notice that the discharge time on C_2 is much slower than the discharge time on C_1.

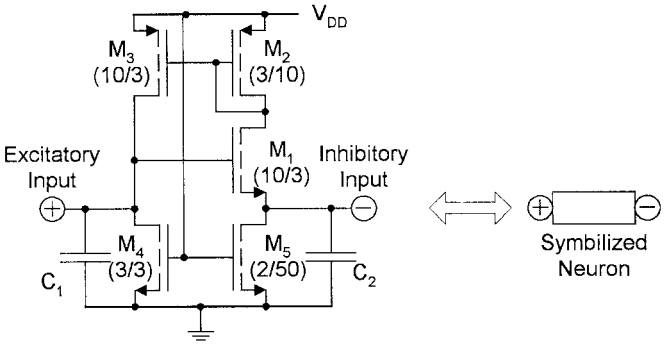


Fig. 3. Actual circuit of neuron cell for CMOS implementation and the symbolized neuron with two input nodes..

refractory period, capacitor C_2 is slowly discharged by resistor R_2, and the neuron cell does not respond to any incoming excitations until the potential on C_1 exceeds the potential on C_2 by the threshold value of M_1. The transient response of the circuit of Fig. 1 for a shifted sinusoidal input excitation is illustrated in Fig. 2. Notice from Fig. 2 that the frequency of output pulses is proportional to the input excitation level; however, the maximum frequency of output oscillation is limited by this refractory period. One can observe this effect with an almost constant frequency for high input excitation level. In actual CMOS implementation, resistors should not be used. Instead, these resistors R_1 and R_2 in Fig. 1 are replaced by transistors M4 and M5, respectively, connected in a diode mode as shown in Fig. 3.

A number of PCNN circuit designs seldom shows the controllability of both excitatory and inhibitory synaptic weights in a complete manner. In order to control both excitatory and inhibitory synaptic weights, the proposed circuit design has two input nodes in the neuron cell—one node at capacitor C_1 for an excitatory (positive) synaptic input, and the other at capacitor C_2 for an inhibitory (negative) synaptic input (Fig. 3). Incoming input currents at the excitatory node are

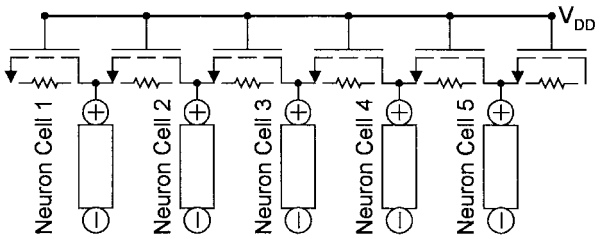


Fig. 4. Neuron cells connected in a chain to form an axon.

charging up capacitor C_1, yielding a positive effect on triggering transistor M_1. Incoming input currents at the inhibitory node are charging up capacitor C_2 which has a negative effect on triggering transistor M_1 by increasing its threshold value. In this scheme both excitatory and inhibitory synaptic weights are controlled, as in natural biological neural networks.

The operation of synaptic weight multiplication in the proposed design can be easily achieved by employing Ohms law. By adjusting the resistance of the coupling resistors, the current, which flows through the axon, is controlled, yielding a corresponding rate of injecting charges into the input capacitor C_1. In the simplest case, NMOS transistors with their gates connected to positive power supply can be used, as Fig. 4 illustrates. In silicon implementation, these coupling resistors are replaced with MOS active resistors. The W/L ratios of such active resistors are adjusted accordingly for synaptic weight multiplication.

III. Neuromorphic Pulse Delay Lines and Properties of Axons

While neural cells in nervous systems are small, their axons for transmitting pulse trains may be very long. Those axons may be coated with myelin sheath, which takes the form of a series of nodes. Myelin is a good insulator, and its layers are far thicker than the membrane. Every few millimeters on a myelinated axon, a bare patch of axon is exposed at what are called nodes of Ranvier [1]. Those nodes of Ranvier create a segmented effect, allowing passage of sodium ions and potassium ions. In addition, the nodes provide a regenerative approach to conduction, providing saltatory conduction to the spiked signal transmission. Nodes are located every few tens of μm, depending on the caliber of the nerve fiber but never more than 300 μm in length, even for newly regenerated fibers which have fewer nodes than undamaged fibers. The inputs of series of neural cells can be connected in a chain by simple coupling resistors to form an axon as shown in Fig. 4. In this section, the following basic properties of axons are emphasized and demonstrated:

1) threshold point of a pulse firing action;
2) pulse shaping action during its propagation through an axon (delay line);
3) refractory period;
4) constant pulse-propagation velocity;
5) annihilation of pulses in case of their collision.

Several researchers have developed a neuromorphic delay lines [4]-[6], [18], [31] demonstrating some of the above properties. Some of these existing designs are compact and attractive, yet some utilize bipolar transistors [4] which consume more power than CMOS counterparts, and an extra synaptic weight control unit is necessary to form a complete neural network [4], [5]. Another interesting design uses a number of CMOS inverters [30] in a single neuron cell to accomplish these properties. The biggest merit of the presented design here is the small number of CMOS transistors with a compact design, allowing less power consumption and reduced silicon area. These five axon properties with the proposed circuitry are discussed in detail here, and the presented equations correspond to the circuit shown in Fig. 3.

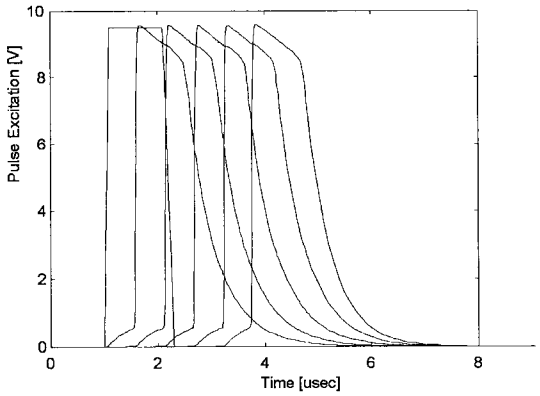


Fig. 5. SPICE simulated transient response to demonstrate the pulse shaping action and constant pulse-propagation velocity from Neuron Cell 1 to Neuron Cell 5 in the axon with a square input voltage.

1) Threshold Point: The first property, threshold point of a pulse firing action, was already demonstrated in Fig. 2 in the previous section. Recall that a pulse is fired when the potential on C_1 exceeds the potential on C_2 by the threshold value of transistor M_1, V_{thM_1}. That is, the condition for the potential on C_1, V_{C1}, to fire a pulse is

$$V_{C1} \geq V_{C2} + V_{thM_1}. \tag{1}$$

2) Pulse Shaping Action: Without a pulse shaping action, traveling pulses could be seriously attenuated and dispersed throughout the transmission. Therefore, axons that have similar membrane structures should be able to regenerate the shape of transmitting pulses. Incoming pulses are regenerated and shaped as they transmit along the axon. Fig. 5 illustrates the pulse shaping action for a square input pulse. If an input pulse is too narrow, it will be annihilated. The shaping of the propagated pulse through the axon depends on the time constant of the output capacitor circuit. Thus, the propagated pulse-duration time $T_{duration}$ is expressed as

$$T_{duration} = C_2\left(\frac{1}{g_{M_1}} + \frac{1}{g_{M_2}}\right) \approx C_2\left(\frac{1}{g_{M_2}}\right) \tag{2}$$

because

$$g_{M_2} \ll g_{M_1}. \tag{3}$$

3) Refractory Period: When the axon circuit is excited with a series of incoming pulses, those pulses can be transmitted through the axon if the incoming pulses are widely separated. On the other hand, some incoming pulses are skipped and not transmitted when the time interval between

the incoming pulses is small. The refractory period of the delay line is caused by significant increase of the threshold voltage at the transistor M_1 after pulse firing. The refractory period $T_{refractory}$, is then expressed in terms of the discharging time of C_2 and the propagated pulse-duration time $T_{duration}$ as

$$\begin{aligned} T_{refractory} &= T_{duration} + T_{rise} + R_{M_5}C_2 \\ &\approx T_{duration} + R_{M_5}C_2 \end{aligned} \tag{4}$$

because

$$T_{rise} \ll T_{duration} + R_{M_5}C_2. \tag{5}$$

4) Constant Pulse-Propagation Velocity: Fig. 5 also demonstrates the property of constant pulse-propagation velocity. Neuron Cell 1 of Fig. 4 is initially stimulated with a voltage input in this simulation. One can observe that the resulting output pulse from Neuron Cell 1 activates Neuron Cell 2 and is seen to propagate at a constant velocity from left to right toward Neuron Cell 5. The extended refractory period of the excited pulses prevents the output pulses of neighboring units from reactivating a previous neural cell and insures that a single pulse is propagated. Constant pulse-propagation velocity in the axon is caused by the delay time T_{delay} of the input pulse, which is applied through the integrating circuit $R_{coupling}C_1$ to each active section of the axon. The delay time is then determined as

$$\begin{aligned} T_{delay} = (R_{M_4}/R_{couple})C_1 \ln\Bigg[1 - V_P\Bigg\{\frac{KW}{2L} \\ \cdot (V_{th} - V_P)^2(R_{M_4}/R_{couple})\Bigg\}^{-1}\Bigg] \end{aligned} \tag{6}$$

where V_P is the transistor pinch-off voltage.

5) Annihilation of Pulses: Annihilation of pulses in case of their collision when pulses are propagating from opposite directions is a consequence of the existence of the refractory period, which causes pulse attenuation. By simultaneously stimulating Neuron Cell 1 and Neuron Cell 5 in Fig. 4, two analog pulses will collide at Neuron Cell 3 and annihilate each other since both Neuron Cell 2 and Neuron Cell 4 will both be in refractory period when Neuron Cell 3 fires a pulse.

IV. Examples

A. Exclusive-OR (XOR)

This example illustrates the functionality of the proposed pulse-coupled neuron circuit design with an exclusive-OR (XOR) function that demonstrates a nonlinear mapping of a set of variables. The network structure with the synaptic weights is shown in Fig. 6. The circuit simulation result for each input pattern is illustrated in Fig. 7. One can observe from this figure that the circuit performs as expected and it follows the nonlinear mapping patterns as required.

B. Image Processing Applications

Biological vision processing appears to require a number of parallel signals, containing color and intensity information, edge enhancement information which is provided by lateral

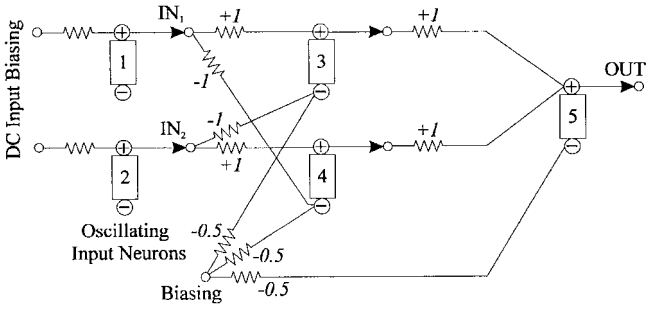


Fig. 6. Network structure of the exclusive-OR example.

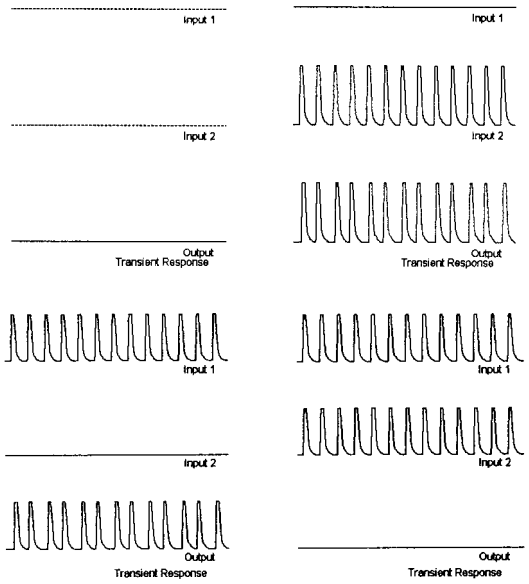


Fig. 7. Voltage waveforms on the outputs of input neurons and the output neuron obtained with SPICE in the exclusive-OR circuit. First two neurons are converting DC voltage input signals into pulse trains. The output pulse train is obtained after the logical exclusive-OR operation.

inhibition between adjacent neurons, Fourier or Gabor filtered information, and others [32]. PCNN's appear to manage combining such a wide variety of information into a coherent process. Eckhorn *et al.* [25] devised an integrate-and-fire neuron model based upon their studies of the visual cortices of cats. The Eckhorn dynamic model represents a visual neuron as a multi-input element with a single output. Most dynamic models of the neural computation suggest that synchronization between regions is the primary information carrier [32]. If time of arrival is used as the information carrier, it demonstrates that mechanism exist in the cellular architectures to perform histogram analysis and adaptive histogram analysis of images [26]. Johnson [27] states that the time signals are unique, object-specific and roughly invariant time signature for their corresponding input spatial image or distribution.

There is one-to-one correspondence between the neurons in the network and the pixels in the image. Therefore, the neuron $N_{i,j}$ in the network corresponds to the pixel $P_{i,j}$ in the image, and vice versa. The key features of image processing with the proposed pulse-coupled neurons are as follows. Suppose that the intensity range of the input image is mapped within [Xmin, Xmax]. The neurons with intensity Xmax fire pulses

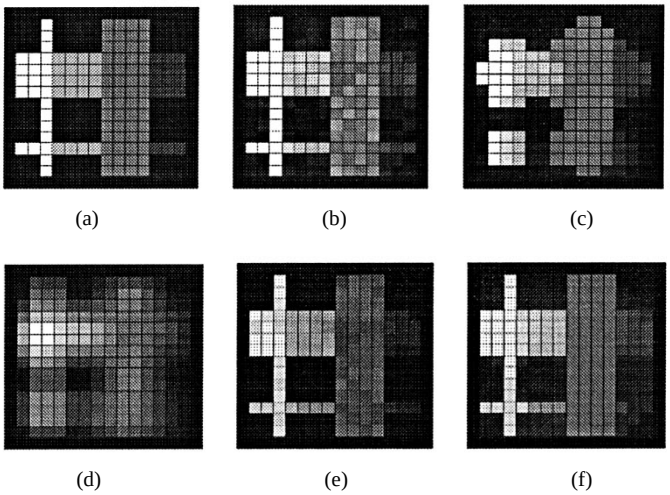


Fig. 8. An example of image filtering and extraction. The original image (a) is added with some random noise (b). The filtered image with a conventional median technique (c) cuts and rounds the corners of the image features. The filtered image with a conventional averaging technique (d) blurs the entire image. Results of PCNN-based image extraction with different neuron coupling coefficients are shown in (e) and (f).

naturally at the highest frequency. This intensity range is referred to as the capture range of $N_{i,j}$ with respect to the group of neurons pulsing at certain time. Then the number of pulses in certain time period is used to extract an image from the time signal back into the corresponding image signal. This image extraction depends on the strength of neuron couplings in the network. This coupling strength, expressed by *neuron coupling coefficient* β of every neuron in the PCNN has the same value β. The following example demonstrates image filtering (or image smoothing) with three different techniques.Neighborhood averaging and median filtering are two commonly utilized techniques.

In general, the intensity of a noisy pixel is significantly different from the intensity of the neighboring pixels. Therefore, the intensity of the noisy pixel is unlikely to lie within its capture range with respect to its neighboring neurons. As a result, the noisy neuron is neither captured by its pulsing neighbors nor captures them. The results of image filtering using these three techniques are shown in Fig. 8. Fig. 8(a) shows the original image without any noise, and Fig. 8(b) is corrupted with additive random noise. The result of filtering the noisy image with the conventional median filtering technique is shown in Fig. 8(c). As it is expected, the corners and edges of the image are eroded and dilated with the median filtering technique. The result of filtering with the averaging technique is blurred, as shown in Fig. 8(d). Figs. 8(e) and 8(f) show the result of filtering the noisy image using the PCNN-based filtering technique with different neuron coupling strength. First, note that PCNN-based filtering does not blur, dilate, or erode the edges of the image. Also, it retains the narrow features in the image significantly well. It is also interesting to observe that the extent of the capture range increases as the neuron coupling coefficient β increases. In other words, a group of pulsing neurons can capture a neuron with considerably lower intensity if a sufficiently large neuron coupling coefficient is used. For this particular example, the neuron coupling coefficient β of 0.01 seems to be a better choice in terms of the image quality.

As can be seen, the capture phenomenon and the capture range play an important role in the image processing applications. That is, the neuron coupling strength determines the neuron synchronization effect. Recall that the coupling between neurons provides a global connection for all subregions in the image, and the neuron coupling enforces global synchrony between local regions.

V. Conclusions

In this paper the CMOS hardware design to realize weighting and summing signals in our pulse-coupled neural network is developed. The proposed neuron circuit has its merits in hardware implementation owing to its simple structure, small size, and high speed of operation, yet achieving all the basic properties of natural biological neurons: 1) threshold point firing; 2) pulse shaping action during its propagation through an axon; 3) refractory period; 4) constant pulse-propagation velocity; and 5) annihilation of pulses in case of their collision. Another important feature of the proposed design is that the circuitry is robust to additive noise. Excitatory and inhibitory synaptic inputs are applied to the two capacitors (two input nodes), C_1 and C_2, respectively, and synaptic weights are adjusted and multiplied by proper W/L ratios of MOS active resistors in axons. The neuron cell circuitry which has been developed here exhibits functional similarities to natural biological neurons through the examples demonstrated in Section IV, and it is highly powerful for image processing applications. It has also been shown that the PCNN has a unique synchronization property.

References

[1] J. A. Anderson, *An Introduction to Neural Networks.* Cambridge, MA: MIT Press, 1995.

[2] S. Deutsch and A. Deutsch, *Understanding the Nervous System: An Engineering Perspective.* Piscataway, NJ: IEEE Press, 1993.

[3] O. H. Schmitt, "Mechanical solution of the equations of nerve impulse propagation," in *Proc. Amer. Physiol. Soc., 49th Annu. Meet.,* Memphis, TN, Apr. 1937.

[4] B. M. Wilamowski, Z. Czarnul, and M. B. Bialko, "Novel inductorless neuristor line," *Electron. Lett.,* vol. 11, no. 15, pp. 355–356, July 24, 1975.

[5] C. Kulkarni-Kohli and R. W. Newcomb, "An integrable MOS neuristor line," *Proc. IEEE,* vol. 65, pp. 1630–1632, Nov. 1976.

[6] A. Hodge, M. Zaghloul, and R. W. Newcomb, "Synchronization of neural-type cells," in *Proc. IEEE Int. Symp. Circuit Syst. (ISCAS),* Atlanta, GA, May 1996, vol. 3, pp. 582–585.

[7] A. F. Murray, D. D. Corso, and L. Tarassenko, "Pulse-stream VLSI neural networks mixing analog and digital techniques," *IEEE Trans. Neural Networks,* vol. 2, pp. 193–204, Mar. 1991.

[8] A. F. Murray and A. V. W. Smith, "Asynchronous VLSI neural networks using pulse-stream arithmetic," *IEEE J. Solid-State Circuits,* vol. 23, pp. 688–697, June 1989.

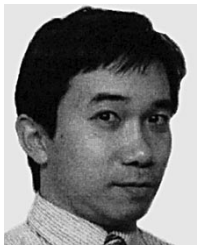
[9] A. Hamilton, A. F. Murray, D. J. Baxter, S. Churcher, H. M. Reekie, and L. Tarassenko, "Integrated pulse stream neural network: Results, issues, and pointers," *IEEE Trans. Neural Networks,* vol. 3, pp. 385–393, May 1992.

[10] G. Moon, M. E. Zaghloul, and R. W. Newcomb, "VLSI implementation of synaptic weighting and summing in pulse coded neural-type cells," *IEEE Trans. Neural Networks,* vol. 3, pp. 394–403, May 1992.

[11] J. L. Meador, A. Wu, C. Cole, N. Nintunze, and P. Chintrakulchai, "Programmable impulse neural circuits," *IEEE Trans. Neural Networks,* vol. 2, pp. 101–109, Jan. 1991.

[12] K. P. Roenker, A. P. Dhawan, and C. K. Song, "Electronic, pulse-mode neural circuits based on a novel semiconductor sevice," in *Proc. Intell.*

Eng. Syst. Through Artificial Neural Net., ANNIE'94 Conf., St. Louis, Nov. 1994, vol. 4, pp. 65–70.
[13] J. Donald and L. A. Akers, "An adaptive neural processing node," *IEEE Trans. Neural Networks*, vol. 4, pp. 413–426, May 1993.
[14] ———, "A neural processing node with on chip learning," in *Proc. IEEE Int. Conf. Circuits Syst.*, Chicago, 1993, pp. 2748.
[15] Y.-C. Kim and M. A. Shanblatt, "Architecture and statistical model of a pulse-mode digital multilayer neural network," *IEEE Trans. Neural Networks*, vol. 6, pp. 1109–1118, Sept. 1995.
[16] B. M. Wilamowski, Y. Ota, and M. L. Padgett, "CMOS realization of pulse-stream artificial neural network using a current controlled oscillator," in *World Congr. Neural Networks*, San Diego, CA, 1996, pp. 1317–1320.
[17] B. M. Wilamowski, M. L. Padgett, and R. C. Jaeger, "Pulse-coupled neurons for image filtering," in *World Congr. Neural Networks*, San Diego, CA, September 15-20, 1996, pp. 851-854..
[18] B. M. Wilamowski, R. C. Jaeger, M. L. Padgett, and L. J. Myers, "CMOS implementation of a pulse-coupled neuron cell," in *Proc. IEEE Int. Conf. Neural Networks*, Washington, D.C., June 1996.
[19] A. F. Murray and L. Tarassenko, *Analogue Neural VLSI: A Pulse Stream Approach.* London, U.K.: Chapman and Hall, 1994.
[20] J. E. Tomberg and K. K. K. Kaski, "Pulse-density modulation technique in VLSI implementation of neural network algorithms," *IEEE J. Solid-State Circuits*, vol. 25, pp. 1277–1286, Oct. 1990.
[21] T. G. Clarkson, C. K. Ng, and Y. Guan, "The pRAM: An adaptive VLSI chip," *IEEE Trans. Neural Networks*, vol. 4, pp. 408–412, May 1993.
[22] M. E. Zaghloul, J. L. Meador, and R. W. Newcomb, *Silicon Implementation of Pulse Coded Neural Networks.* Norwell, MA: Kluwer, 1994.
[23] J. J. Hopfield, "Neural networks and physical systems with graded response have collective properties like those of two-state neurons," in *Proc. Nat. Academy Sci., USA*, May 1984, vol. 81, pp. 3088–3092.
[24] M. L. Padgett, P. J. Werbos, and T. Kohonen, "Strategies and tactics for the application of neural networks in industrial electronics," *CRC Handbook for Industrial Electronics*, J. D. Irwin, Ed. Boca Raton, FL: CRC Press/IEEE Press, 1996.
[25] R. Eckhorn, H. J. Reitboeck, M. Arndt, and P. Dicke, "Feature linking via synchronization among distributed assemblies: Simulations of results from cat visual cortex," *Neural Comput.*, vol. 2, pp. 293–307, 1990.
[26] G. Tarr, R. Carreras, C. Dehainaut, X. Clastres, L. Freyss, and M. Samuelides, "Intelligent sensors research using pulsed coupled neural networks for focal plane image processing," in *Proc. Applicat. Sci. Artificial Neural Networks II*, Orlando, FL, Apr. 1996, vol. 2760, pp. 534–542.
[27] J. L. Johnson, "Pulse-coupled neural networks," in *Proc. Adaptive Computing: Mathematics, Electronics, and Optics*, S.-S. Chen and H. J. Caulfield, Eds., Orlando, FL, Apr. 1994, vol. CR55, pp. 47–76.
[28] H. S. Ranganath and G. Kuntimad, "Iterative segmentation using pulse coupled neural networks," in *Proc. Applicat. Sci. Artificial Neural Networks II*, Orlando, FL, Apr. 1996, vol. 2760, pp. 543–554.
[29] J. Kinser and H. J. Caulfield, "An O(N0) pulse-coupled neural network performing human-like logic," in *Proc. Applicat. Sci. Artificial Neural Networks II*, Orlando, FL, Apr. 1996, vol. 2760, pp. 555–562.
[30] W. Yang, "Neuromorphic CMOS circuitry for active bidirectional delay lines," in *Proc. IEEE Int. Symp. Circuit Syst. (ISCAS)*, Atlanta, GA, May 1996, vol. 3, pp. 473–477.
[31] Special issue of IEEE SPECTRUM, pp. 20-69, May 1996.
[32] A. K. Gray, C. M. Konig, P. Engel, and W. Singer, "Stimulus-dependent neural oscillations in the cat visual cortex exhibit intercolumnar synchronization which reflects global stimulus properties," *Nature*, vol. 338, pp. 334–337, 1989.



Yasuhiro Ota He received the B.S., M.S., and Ph.D. degrees in electrical engineering from the University of Wyoming, Laramie, in 1991, 1993, and 1996, respectively.

His research interests include VLSI implementations of pulse-coupled neural networks and fuzzy logic controllers, robotics, and control systems. He has published 15 articles in refereed journals and conference proceedings since his graduate studies. Currently Dr. Ota is with Minolta Corporation in Japan, and extends his research and development in ASIC designs for digital color image processing units.

Bogdan M. Wilamowski (SM'83) received the M.S. degree in computer engineering in 1966, the Ph.D. in electrical engineering in 1970, and D.Sc. in VLSI electronics in 1977, all from Technical University of Gdansk, Poland.

He was the Director of the Institute of Electronic Technology from 1979–1981 and during 1988–1989, he was the Head of the Solid State Electronic Chair at this University. From 1968 to 1970, and in 1975–1976 he was with the Nishizawa Laboratory at Tohoku University, Japan. During 1981–1982 and 1995–1996 he was with Auburn University, and during 1982–1984, he was with the University of Arizona, Tucson. Since 1989, he has been with the University of Wyoming. He is the author of three books, more than 190 refereed publications, and 27 patents.

Dr. Wilamowski is currently the member of IEEE Neural Network Council, Associate Editor of the IEEE TRANSACTIONS ON NEURAL NETWORKS, and an officer of IEEE Industrial Electronics Society.