BURIED-CHANNEL MOS TRANSISTOR WITH PUNCH-THROUGH

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Abstract—The punch-through phenomenon is normally considered as a parasitic mechanism in MOS devices, which is critical for short channel MOS transistors. An MOS transistor operation in the presence of punch-through is studied in this paper. A proper device geometry and additional substrate biasing enable useful voltage gain of the transistor, even if the punch-through is the dominant mechanism. Principle of operation and experimental data of the MOS controlled punch-through transistor is presented.

INTRODUCTION

The semiconductor device with carrier injection over an electrostatically induced potential barrier, named the Static Induction Transistor (SIT), was invented by Nishizawa et al. [1]. A very similar concept using GaAs Schottky gate is known as the permeable base transistor [2, 3]. These types of transistors operate with opposite polarity of gate and drain voltages and, therefore, they have limited applications for digital circuits. Also, their structures are not very suitable for integration in general. However, using the bipolar mode of SIT and 5 μm photolithography rules, the integrated logic with power-delay product of 0.002 pJ is reported [4, 5]. This logic structure is very sensitive to the fabrication parameters [6, 7]. The concept with the MOS gate controlled SIT structure is also proposed by Nishizawa [8]. The assumption was that the gate threshold voltage can be shifted using, e.g., the ion implantation technique. Charge accumulation under MOS gate is the main problem there, so the electrical field penetration is very shallow. Even for very high gate voltages, it is not possible to turn the device off. Using the tetrode structure with two gates, a MOS and a junction one, it seems possible to overcome this difficulty. The study of such a structure is covered in this paper.

Analysis and experiment of a MOS tetrode was already published by Richman [9], but this device was considered mainly as a MOS transistor with the substrate being the fourth electrode. Also, similar structures were recently described as buried or subsurface MOS transistors [10–14]; however, these transistors operate as a junction FET with a long channel. In the case of the device described here, the buried channel transistor operates in the punch-through and the space-charge-limited mode. This device is similar to the planar structure of lateral punch-through transistor published recently [15]. However, instead of the gate made by the impurity diffusion, the gate is formed with the surface region inverted by the voltage applied to the MOS gate. This structure, contrary to the lateral punch through transistor where the gate is shorted to the substrate, is suitable for integration.

DEVICE STRUCTURE

The basic device structure is shown in Fig. 1. Two MOS transistors, one with a p-type channel and the other with a n-type one, share a common gate but have perpendicular channels. The n-type surface channel of one of these transistors acts as a gate for the other transistor with the p-type buried channel.

![Fig. 1. The buried punch-through MOS transistor: (a) top view, (b) cross section of the n-channel surface device, (c) cross section of the p-channel buried punch-through device.](image_url)
This buried p-type channel transistor operates in a punch-through mode. During normal operation, the source and drain of the n-type surface channel transistor are shorted to n-type substrate and connected to a positive voltage. The source of the p-type buried transistor is grounded, and drain is connected to a negative voltage. The equivalent circuit of this device for the purpose of analysis is shown in Fig. 2.

For various voltages of the MOS gate, the device has different modes of operation (Fig. 3). For positive voltage on the MOS gate, the n-type region is induced near the surface (Fig. 3a). This n-type region with positive biasing operates as a gate, similar to the gate of the lateral punch-through transistor[15]. If a negative voltage is applied to the MOS gate, the surface will be inverted to the p-type and the punch-through current will flow for relatively small voltages between the p-type source and drain. In addition to the punch-through current, the current in the p-type surface channel may also flow (Fig. 3b). The device will operate in the accumulation punch-through mode[16, 17].

**Fig. 2.** The equivalent circuit of buried punch-through MOS structure.

**Fig. 3.** Two modes of operation of a buried transistor: (a) punch-through mode, (b) accumulation and punch-through mode.

**EXPERIMENT**

First, two buried p-type device structures with different geometry were fabricated. The fabrication facilities limit the size of devices to relatively large ones. Therefore, in order to observe the desired effects, low substrate background impurity concentration with high resistivity (600 Ω-cm) was chosen. Device No. 1 had a source-drain spacing equal to 7.5 μm covered by the MOS gate. The source-drain spacing in device No. 2 was 10 μm and only half of this region at the source side was covered by the MOS gate (Fig. 4).

The drain current of device No. 2 as a function of drain voltage for various junctions, and MOS-gate-biasing is shown in Figs. 5 and 6 using linear and logarithmic scales, respectively. These characteristics are very similar to those of the lateral punch-through

**Fig. 4.** The cross section of fabricated devices: (a) device No. 1 with 7.5 μm source-drain spacing, (b) device No. 2 with 10 μm spacing and partly covered channel.

**Fig. 5.** The drain characteristics of device No. 2 with the MOS gate voltages equal to +15, 0, −15 V and the n-type junction gate voltages varying from 0 to 10 V (2 V per step). For MOS gate voltage equal to −15 V, the junction gate biasing has only small effect on the device characteristics.
mode of operation. For highly negative voltages on the MOS gate, the p-type channel with hole accumulation exists near the surface, and punch-through voltage between this p-type surface channel and p-type drain is relatively small. Higher values of junction gate potentials have almost no effect on the punch-through voltages. This mode of operation is illustrated in Fig. 3(b). For highly positive voltages applied to the MOS gate, the surface is inverted to the n-type region which is internally connected with the junction gate. Voltages of the junction gate have significant effects on the drain current. The terminal voltages induce a potential barrier whose height is controlled both by the applied voltages to the junction gate and drain and also by the carrier space-charge, which is proportional to the current density. This mode of operation is illustrated in Fig. 3(a) and is very similar to the one described in [15]. In the case of device No. 1 where the MOS gate covers the whole region between source and drain, the effect of the junction gate was smaller (Fig. 8).

These two modes of transistor action also can be observed on the gate characteristics for fixed drain voltage. Such characteristics of device No. 2 are shown in Fig. 9. For negative voltages on the MOS gate, the drain current is independent on the junction gate voltage when the MOS gate controls the accumulation space-charge-limited drain current Fig. 3(b)[9, 16, 17]. In the case where positive voltage is applied to the MOS gate, the n-type region is induced under MOS gate and the device operation is similar to those of the lateral punch-through transistor[15].

A similar behaviour was observed by Richman[9], but the induced gate was not mentioned and the results were interpreted as an effect of substrate interaction. In order to investigate this substrate
Fig. 9. The MOS gate characteristics of device No. 2 with the n-type junction gate voltages as parameters and the fixed-drain voltage equal 40 V.

![Diagram of MOS gate characteristics](image)

Fig. 10. The top view of device No. 3.

In this paper, the problem of MOS transistor operation in the presence of punch-through was studied. Special device modifications and additional biasing causes a useful gain, even if the punch-through phenomenon is present. A small transit time (large electrical field) and small parasitic capacitances (small substrate impurity concentration) are advantages of this device. In measured devices, the voltage gain was relatively small, usually not more than two. However, further device geometry modifications may improve this parameter.

One of the disadvantages of this structure is that the additional biasing of the junction gate (substrate) is necessary. However, current requirements for such additional biasing are very small. Also, for high speed applications, the effect of series resistance between junction gate and enhancement region under MOS gate should be studied.

REFERENCES

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Buried channel MOS transistor with punch-through


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MOS transistor structure is that of a p-n junction, with the a-substrate forming a p-n junction with the drain drain. The punch-through phenomenon is observed in these devices, where the punch-through capacitance is significant. The punch-through capacitance is a function of the drain voltage and the substrate doping. The punch-through capacitance is minimized by using a high substrate doping and a low drain voltage. The punch-through capacitance is also affected by the drain current, with higher drain currents resulting in higher punch-through capacitances. The punch-through capacitance is minimized by using a low drain current.

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d voltage in the range of 3 V to 5 V for the n-type substrate with the a-substrate being the p-type substrate. The punch-through capacitance is a function of the drain voltage and the substrate doping. The punch-through capacitance is minimized by using a high substrate doping and a low drain voltage. The punch-through capacitance is also affected by the drain current, with higher drain currents resulting in higher punch-through capacitances. The punch-through capacitance is minimized by using a low drain current.

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