DIGITAL INTEGRATED CIRCUIT TRANSIENT ANALYSIS PROGRAM

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ABSTRACT

A program for transient analysis of very large digital integrated circuits, based on a charge conservation principle, (SPICE2), is described. A developed relatively simple explicit algorithm over the scheme of the conduction currents at each node to compute the charge stored on capacitances connected to each node.

The program is oriented on digital HST circuits and is suitable only to transient analysis. A variety of circuits ranging from simple inverter to ring oscillators, transmission gates and flip-flops have been analyzed. For multi-complexity bipolar circuits, the CPU time is similar to those needed for the SPICE2 circuit simulation program. However, for HST circuits even with the increased complexity, the computing time is significantly shorter (10-100 times for a medium size HST circuit, depending on accuracy of solution).

1. INTRODUCTION

To improve the computing speed of CDS tools, various approaches are used, such as sparse matrix techniques, implicit integration methods, a sparse tableau analysis method, a modified nodal analysis method, circuit decomposition or a modular approach e.g. [11,12,13]. Also a waveform relaxation method [4], which takes advantage of signal latency requires a very large memory and, in the case of circuits with many feedback loops, its efficiency is rather poor. A method to compress storage data by one or two orders of magnitude has recently been published [15].

In this paper, we describe a simple explicit method in which the computing time for HST medium-size circuits is up to 10-100 times shorter than required by the SPICE2 program [14,17], the higher number being for the default values of optional parameters of SPICE2, which were used to obtain the required accuracy. SPICE2 is used here to check the accuracy of our solutions, and as a reference only for speed comparison.

2. PRINCIPLES OF THE ALGORITHM

At any node of the circuit consisting of nonlinear resistors, sources and capacitors, displacement current must flow if the algebraic sum of conduction currents flowing into a node is not zero. These displacement currents result from the charging of capacitances connected to the node. In general, a set of nonlinear differential equations must be solved.
\[ I_{1j}(t) + C_{ij}(v_j) \frac{dv_j}{dt} = 0 \]

\[ I_{1j}(t) + C_{ij}(v_j) \frac{dv_j}{dt} = 0 \]  \hspace{2cm} (1)

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statements: \( I_{1j}(t) \) are the conduction currents flowing into node \( j \), \( C_{ij}(v_j) \) are nonlinear functions of voltage, \( v_{ij} \) are voltages between nodes \( i \) and \( j \), and \( n \) is the total number of nodes.

If it is assumed that all voltages are known, the values of all conduction currents can be calculated. The net conduction current \( I_{1j} \) flowing into a node \( j \) for an interval \( dt \) produces a charge increment \( Q_{1j} = I_{1j} dt \), which is distributed among the capacitances connected to the node. In an integrated circuit, the capacitances are nonlinear functions of node voltages, and conduction currents. Thus, if the node voltages are known, the capacitances can be calculated. Then, a network of capacitors of known capacitance can be analyzed with the previously calculated value of \( Q_{1j} \) at each node: from this the corresponding \( v_j \) at each node can be determined. For the next time interval, the node voltages are incremented by their appropriate \( Q_{1j} \)'s. Now \( I_{1j}, Q_{1j} \), and \( v_{ij} \) are then calculated.

The algorithm is then implemented as follows:

1. If initial node voltages are not known, assume plausible values (perhaps 0) and compute the net conduction current at each node:

\[ I_{1j} = \sum_{j=1}^{N} I_{1j}^{(0)} \]  \hspace{2cm} (2)

where the summation indicates that there are \( K \) conduction currents flowing into node \( j \). Note that there may be nonlinear functions of various node voltages.

In the static case, the \( I_{1j} \) are, of course, all zero.

2. Calculate for each node the charge increment accumulated during \( dt \):

\[ Q_{1j} = I_{1j} dt \]  \hspace{2cm} (3)

3. Since the functions \( I_{1j}(v) \) are generally unknown, and only discrete values for the previous time steps are available, the slope of this function can be predicted using zero, first or second order interpolations, respectively:

with the zero order interpolation:

\[ Q_{1j} = \alpha_t \cdot I_{1j}(t) \]  \hspace{2cm} (4)

with the first order interpolation:

\[ Q_{1j} = \alpha_t \cdot (1.5 I_{1j}(t) - 0.5 I_{1j}(t - dt)) \]  \hspace{2cm} (5)

with the second order interpolation:

\[ Q_{1j} = \alpha_t \cdot (1.75 I_{1j}(t) - 1.75 I_{1j}(t - dt)) \]  \hspace{2cm} (6)

In the last case, values from two previous time periods must be stored. In general, for the zero-order case, very short time steps must be used to achieve the required accuracy. As a compromise, the first-order case was used in examples to be given.

3. Using an appropriate interpolation method, predict the values of all nonlinear capacitances for the time \( t + dt \). For example, with the first order interpolation:

\[ C(t + dt) = C(t) + Q_{1j} \]  \hspace{2cm} (7)

4. Compute \( Q_{1j} \) at each node. Since \( Q_{1j} \) are known, \( t \) are the capacitance values of all capacitors, the following set of equations representing the network must be solved:

\[ C_{1j} v_j + \sum_{j=1}^{N} C_{ij}(v_j - v_i) = Q_{1j} \]

\[ C_{1j} v_j + \sum_{j=1}^{N} C_{ij}(v_j - v_i) = Q_{1j} \]  \hspace{2cm} (8)

\[ C_{1j} v_j + \sum_{j=1}^{N} C_{ij}(v_j - v_i) = Q_{1j} \]

\[ C_{1j} v_j + \sum_{j=1}^{N} C_{ij}(v_j - v_i) = Q_{1j} \]
where: $C_{ij}$, $C_{ij}^{1}$ are interpolated values of intercond and coupling capacitances, and $V_{ij}$, $V_{ij}^{1}$ are increments of node voltages caused by the change in current $I_{ij}$.

Note that if there are $B$ nodes, Eq. (10) represents a system of $B$ linear equations. Solution of these equations is discussed in the next section.

5. Compute the new values of nodal voltages.

$$V_{i}^{(k+1)} = V_{i}^{(k)} + \Delta V_{i}$$

(9)

In the implementation of the algorithm, the time period of interest, $t$, is divided into subintervals called external time steps. Data points are to be calculated at each external time step. The external time steps are divided into intervals called internal time steps. An iterative procedure using the internal time steps is carried out to obtain convergence for each external time step.

3. SOLUTION OF THE COEFFICIENT MATRIX

As was discussed in step 4 of the algorithm, to compute $V_{i}$ a network of capacitances must be analyzed. Such a network is characterized by a matrix equation in the general form:

$$[C_{ij}^{1}] \cdot [V_{i}] = [V_{ij}]$$

(10)

Since the capacitance values for a given time interval are held constant, Eq. (10) is linear. Moreover, since the capacitive network is passive, the main diagonal of the $C_{ij}$ matrix is always dominant. Therefore, a simple Gauss-Seidel iterative procedure can be applied, and convergence is guaranteed.

In many cases, the ground capacitances are dominant, and convergence is very rapid. In examples that have been analyzed with the Gauss-Seidel procedure, convergence was typically obtained in 10 to 20 iterations when the ground capacitances were dominant. However, convergence is slow in cases where large capacitances between nodes occur. As an example, consider the circuit of Fig. 1. In this case, the capacitances between nodes are up to 100 times greater than the ground capacitances, and convergence was not obtained even after 1000 iterations; this is illustrated in Fig. 7.

A method producing a more rapid convergence assumes an exponential relationship for the node voltage increments:

$$V_{i}^{(k+1)} = V_{i}^{(k)} + \Delta V_{i}^{(k)}$$

(11)

$$\Delta V_{i}^{(k)} = V_{i}^{(k)} - V_{i}^{(k-1)}$$

(12)

Therefore, after a few steps of using the standard Gauss-Seidel iterative procedure, new predicted values of node voltages can be computed such as the k-th step. Fig. 3 shows that, even for networks with large capacitances between nodes (Fig. 1), rapid convergence is obtained.

6. SIMULATION OF BIPOLAR INTEGRATED CIRCUITS

To test the algorithm, a cascade of 4 bipolar inverter stages shown in Fig. 4 was analyzed. Such a saturating type of circuit has very nonlinear capacitances. The equivalent circuit for the bipolar transistors is shown in Fig. 5; functional dependences of the nonlinearities are given in Table 1.

Figure 6 shows the computed waveforms for the node voltages at a time increment of 1 nsec and total time period of 100 nsec. Note that there are no differences between the figures. All computations were performed on a WAX-11/380 computer; for our algorithm the CPU time was 9.10 seconds while with SPACE2 it was 23.66 seconds. The times are not very different due to the fact that the circuit contains large highly nonlinear capacitances which are not grounded and also static characteristics of bipolar transistors are very nonlinear in nature. Thus, the explicit algorithm does not have significant advantage over the implicit method used in SPACE2. In order to secure convergence for this particular circuit, the internal time step was 12 times smaller than the external time step of 1 nsec. In other words, the maximum possible internal time increment in computing the algorithm was 0.08 nsec. For larger internal time steps, convergence was not obtained.

5. SIMULATION OF MOS INTEGRATED CIRCUITS

The method described herein is more suitable for simulation of MOS circuits than bipolar circuits because the nonlinearities in the former are less severe. A cascade of 7 MOS inverters shown in Fig. 8 was analyzed. The device
Further reduction of CPU can be expected if means are used to take advantage of signal latency (temporary quiescence). The algorithm is so structured that it is relatively simple to omit computation at inactive nodes when this is warranted.

REFERENCES


Fig. 1. Example of capacitive circuit activated by voltage source applied to node 9 and by injected charges into nodes 1 and 2.

Fig. 2. Node voltage increments $v_n$ for the circuit shown in Fig. 1 as a function of iteration of a Gauss-Seidel algorithm.

Fig. 3. Node voltage increments $v_n$ for the circuit shown in Fig. 1 as a function of iteration of a modified Gauss-Seidel algorithm.

Fig. 4. Bipolar circuit analyzed with Gnod and SPICE programs.

Fig. 5. Equivalent circuit for the bipolar BHI transistor model used in Gnod.

$I_{CE} = I_{RB} + \exp(V_{BE}/V_T) - 1 + 1/I_{RB}$

$I_{CB} = I_{RB} + \exp(V_{BE}/V_T) - 1 + 1/I_{RB}$

$I_B = I_{CF} + I_{CR}$

$I_C = I_{CE} + I_{RB} + I_{CR}$

$I_{CE} = I_{CE} + I_{RB} + I_{CR}$

$I_{BE} = I_{RB} - V_T / V_B + V_T / V_B$

$I_{BE} = I_{RB} - V_T / V_B + V_T / V_B$

$I_{CE} = I_{CE} + I_{RB} + I_{CR}$

$I_{CR} = I_{CR} + I_{RB} + I_{CR}$

Table 1. Functional dependence of BHI bipolar transistor model.
Fig. 8. Cascade of 7 MOS inverters analyzed with QWID and SPICE programs.

Fig. 9. Equivalent circuit for the N-channel MOS transistor used in QWID.

Table 2. Functional dependence of N-channel MOS transistor parameters.
Fig. 10. Computed waveforms of the node voltages for the circuit of Fig. 8 obtained with program SPICE.

Fig. 11. Computed waveforms of the node voltages for the circuit of Fig. 8 obtained with program SPICE.

Fig. 12. Block diagram of the circuit containing 16 CMOS inverters for analysis with GEnetic program.

Fig. 13. Computed waveforms of some of node voltages for the circuit of Fig. 12.
Table 1.

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A METHODOLOGICAL APPROACH TO THE OPTIMIZATION OF VOLTAGE QUALITY IN DISTRIBUTION NETWORKS

G. CARPINELLO - R. MONGELLA \& A. TESI (**) \*

Abstract. The problem of the optimal choice of the transformer ratios in a radial distribution network is considered. The optimal condition is assumed to be the one minimizing a function of the voltage deviation costs. Resolution approaches are proposed taking into account the discretization of the problem variables. The situations that can occur both in public and industrial distribution networks are considered.

List of principal symbols:

- H: number of branches (substation transformers);
- m: number of the second's substations transformers;
- u: number of the taps in the HV/LV substation transformer;
- v: number of the taps in the MV/LV secondary substation transformer;
- D: costs caused by low voltage deviations;
- α: cost coefficient;
- Di, bj: diagonal matrix whose elements along the diagonal are the components of the vector [L];
- [P]T: column vector of the branch powers and reactions, respectively;
- [A]T: network topological matrix;
- [L]T: transpose of the matrix [L];
- [I]T: column vectors of the load active and reactive powers, respectively;
- [P]T, [Q]T: column vectors of the branch active and reactive powers, respectively;
- [ΔV]t: column vector of the branch voltage drops;
- [ΔV]t: column vector of the total voltage drops between the supplying node and the load nodes;
- α: HV/LV transformer ratio;
- β: ratio of the 4th MV/LV transformer;
- γ: HV/LV transformer ratio which minimizes the costs.

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