Field Programmable Gate Arrays

- Configuration Memory
- Programmable Logic Blocks (PLBs)
- Programmable Input/Output Cells
- Programmable Interconnect

Typical Complexity = 5M – 1B transistors
Basic FPGA Operation

Write Configuration Memory
- Defines system function
  - Input/Output Cells
  - Logic in PLBs
  - Connections between PLBs & I/O cells

Changing configuration memory data => changes system function
- Can change at anytime
  - Even while system function is in operation
  - Run-time reconfiguration (RTR)
Basic PLB Architecture

- Look-up Table (LUT) implements truth table
- Memory elements:
  - Flip-flop/latch
  - Some FPGAs - LUTs can also implement small RAMs
- Carry & control logic implements fast adders/subtractors
A Simple PLB

- Two 3-input LUTs
  - Can implement any 4-input combinational logic function
- 1 flip-flop
  - Programmable:
    - Active levels
    - Clock edge
    - Set/reset
- 22 configuration memory bits
  - 8 per LUT
    - C0-7
    - S0-7
  - 6 controls
    - CB0-7

![Diagram of a simple PLB with LUTs and flip-flops]
Combinational Logic Functions

- Gates are combined to create complex circuits
- Multiplexer example
  - If S = 0, Z = A
  - If S = 1, Z = B
  - Very common digital circuit
  - Heavily used in FPGAs
    - S input controlled by configuration memory bit
    - We’ll see it again
Look-up Tables

- Recall multiplexer example
- Configuration memory holds outputs for truth table
- Internal signals connect to control signals of multiplexers to select value of truth table for any given input value
Look-up Table Based RAMs

- Normal LUT mode performs read operations
- Address decoder with write enable generates clock signals to latches for write operations
- Small RAMs but can be combined for larger RAMs
Example PLB

- 1/4 of a PLB (called a slice) from Xilinx Spartan 3
  - Two 4-input Look-Up Tables (LUTs)
    - Can perform any combinational logic function of up to 4 inputs
    - Can function as small RAM (16x1-bit) or shift register (up to 16-bit)
  - Two D-type flip-flops
    - Programmable as level sensitive latches
    - Programmable clock edge, clock enable, set/reset
  - Extra logic
    - Fast carry for adders
    - MUXs for Shannon expansion
    - And more
Spartan 3 PLB Slices
Interconnect Network

• Wire segments of varying length
  – $xN = N$ PLBs in length
    • 1, 2, 4, 6, and 8 are most common
  – $xH = \text{half the array in length}$
  – $xL = \text{length of full array}$

• Programmable Interconnect Points (PIPs)
  • Also known as Configurable Interconnect Points (CIPs)
  – Transmission gate connects to 2 wire segments
  – Controlled by configuration memory bit
    • 0 = wires disconnected
    • 1 = wires connected
PIPs

- **Break-point PIP**
  - Connect or isolate 2 wire segments
- **Cross-point PIP**
  - Turn corners
- **Compound cross-point PIP**
  - Collection of 6 break-point PIPs
    - Can route to two isolated signal nets
- **Multiplexer PIP**
  - Directional and buffered
  - Select 1-of-N inputs for output
    - Decoded MUX PIP – N config bits select from $2^N$ inputs
    - Non-decoded MUX PIP – 1 config bit per input
PLB consists of 4 slices over 2,400 PIPs mostly MUX PIPs. The switch matrix consists of x6 wire segments, x2 wire segments, xH & xL wire segments, over 450 total wire segments in PLB.
Input/Output Cells

• Bi-directional buffers
  – Programmable for input or output
  – Tri-state control for bi-directional operation
  – Flip-flops/latches for improved timing
    • Set-up and hold times
    • Clock-to-output delay
  – Pull-up/down resistors

• Routing resources
  – Connections to core of array

• Programmable I/O voltage & current levels
FPGAs

• Recent trend - incorporate specialized cores
  – RAMs – single-port, dual-port, FIFOs
    • 128 bits to 36K bits per RAM
    • 4 to 575 per FPGA
  – DSPs – 18x18-bit multiplier, 48-bit accumulator, etc.
    • up to 512 per FPGA
  – Microprocessors and/or microcontrollers
    • up to 2 per FPGA
      – Hard core processor
    • Support soft core processors
      – Synthesized from HDL into programmable resources
Specialized Cores

Virtex and Spartan II

Virtex II and Spartan 3

4K-bit RAMs

18K-bit RAMs and 18×18-bit multipliers

RAMs/multipliers

2S15 2S30 2S50 2S100 2S150 2S200 2V40 2V80 2V250 2V500 2V1000 2V1500 2V2000 2V4000 2V6000 2V8000 2VP2 2VP4 2VP7 2VP20 2VP40 2VP50 2VP70 2VX100
Spartan 3 Programmable RAMs

- 18 Kbit dual-port RAM
- Each port independently configurable as
  - 512 words x 36 bits
    - 32 data bits + 4 parity bits
  - 1K words x 18 bits
    - 16 data bits + 2 parity bits
  - 2K words x 9 bits
    - 8 data bits + 1 parity bit
  - 4K words x 4 bits (no parity)
  - 8K words x 2 bits (no parity)
  - 16K words x 1 bit (no parity)
- Each port has independently programmable
  - clock edge
  - active levels for write enable, RAM enable, reset
Spartan 3 (XC3S200)

- PLBs = 24 rows x 20 columns = 480
  - 4 slices/PLB
    - 2 L slices
      - L = logic
    - 2 M slices
      - M = memory
- RAMs = 12
  18Kbit dual port RAMs
- Multipliers = 12
  18x18-bit signed
# Ranges of Resources

<table>
<thead>
<tr>
<th>FPGA Resource</th>
<th>Small FPGA</th>
<th>Large FPGA</th>
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<tbody>
<tr>
<td>Logic</td>
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<tr>
<td>PLBs per FPGA</td>
<td>256</td>
<td>25,920</td>
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<tr>
<td>LUTs and flip-flops per PLB</td>
<td>1</td>
<td>8</td>
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<td>Routing</td>
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<tr>
<td>Wire segments per PLB</td>
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<td>PIPs per PLB</td>
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<td>Specialized Cores</td>
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<tr>
<td>Bits per memory core</td>
<td>128</td>
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<tr>
<td>Memory cores per FPGA</td>
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<tr>
<td>DSP cores</td>
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<td>Other</td>
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<tr>
<td>Input/output cells</td>
<td>62</td>
<td>1,200</td>
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<tr>
<td>Configuration memory bits</td>
<td>42,104</td>
<td>79,704,832</td>
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</tbody>
</table>
Xilinx FPGAs

- Virtex and Spartan 2
  - Array of 96 to 6,144 PLBs
    - 4 LUTs/RAMs (4-input)
    - 4 FF/latches
    - 4 to 32 4K-bit dual-port RAMs
- Virtex II, Virtex II Pro
  - Array of 352 to 11,204 PLBs
    - 8 LUTs/RAMs (4-input)
    - 8 FF/latches
    - 12 to 444 18K-bit dual-port RAMs
    - 12 to 444 18×18-bit multipliers
    - 0 to 2 PowerPC processor cores
- Virtex 4
  - Array of 1,536 to 22,272 PLBs
    - 4 LUTs/RAMs (4-input)
    - 8 FF/latches
    - 48 to 552 18K-bit dual-port RAMs
      - Also operate as FIFOs
    - 32 to 512 DSP cores include:
      - 0 to 2 PowerPC processor cores
- Spartan 3
  - Array of 192 to 8,320 PLBs
    - 4 LUTs/RAMs (4-input)
    - 4 LUTs (4-input)
    - 8 FF/latches
    - 480–3S200
      - 4 to 104 18K-bit dual-port RAMs
      - 4 to 104 18×18-bit multipliers