Multi-Mode Scan:  
Test-per-Clock BIST for IP Cores

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Scan Based Logic BIST
- Industry Standard

LSFR
Linear Feedback Shift Register

Random Pattern Generation → Scan Flip Flops → Result Compression

SISA (MISA)
Single/Multiple Input Signature Analyzer
Scan Based Logic BIST

>>> Attractive solution for Core test

- Minimal need for test access busses
  - Can be supported by IEEE 1149.1

- Can run complete BIST test as specified by the core provider (for “hard” cores)
  - Fault Simulations models are not needed by SoC integrator

>>> Protects IP
Scan Based Logic BIST

Two serious limitations:

- Slow test-per-scan test execution
- Very limited support for two/multiple vector delay tests
Multi-Mode Scan: *Test-per-Clock BIST*

- Employs Circular BIST
- Combines test generation/results compression in FFs

- Retains ALL benefits of scan based logic BIST

- Fast test-per-clock operation
  > 2 orders of magnitude faster

- Many other advantages

![Diagram of Multi-Mode Scan: Test-per-Clock BIST](image)
Circular BIST

The Basic Idea:

- Suppose we scan in a random state into the circuit flip-flops as an initial state

- Now if we EXOR the next circuit state with this shifted random initial state, we will essentially get another random state vector
Circular Self Test Path (CSTP)

Fig. 6. Circular Self Test Path Memory Element[10]
Pseudorandom Circular Self-Test
Circular Self Test Path (CSTP)

Fig. 6. Circular Self Test Path Memory Element[10]
Overview of Circular BIST

• Replace existing flip-flops with CBIST flip-flops
• Connect CBIST flip-flops to form circular chain
• Isolate system data inputs for reproducible results
• Add test controller to control BIST sequence
  – Initialization
  – BIST mode
  – Read signature
  – Return to system mode

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<td>Di ⊕ Qi-1</td>
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Circular BIST Flip-Flop & Modes
Overview of Circular BIST

- Easy to create CAD tools for BIST synthesis
- *Vertical testability* (from wafer to system level)
- High fault coverage (typically > 90%)
- Scan mode for augmenting fault coverage
- At-speed testing
- Low area & performance penalties
  - typically 10% to 20% additional logic
  - 2 to 3 gate delays
  - Control by selective replacement
- Also known as Circular Self-Test Path (CSTP)
Problems with Circular BIST

- Low fault coverage in some circuits due to:
  - Register adjacency
    - Worst when \( D_i = Q_{i-1} \) then \( Z_i \) is always logic 0
    - Can occur whenever \( D_i = f(Q_{i-1}) \)
    - Compacted data containing fault information is lost unless the bit(s) can propagate through the circuitry under test
    - Avoid by ordering CBIST chain
  - Limit cycling
    - Due to the closed nature of CUT in BIST mode
    - Also function of initialization state
Register Adjacency
Limit Cycling in Circular BIST

- Cycle length of BIST sequence is a function of:
  - Initialization value
  - State Transition Graph
- Once a loop is entered, the sequence repeats
- Head states can maximize cycle length (Prinetto et.al., ITC’94)
- Circuit under test may never visit all states
- Few state transitions => few test patterns => low fault coverage
Multi-Mode Scan: *Test-per-Clock* BIST

- Combines test generation/results compression in FFs

- Retains ALL benefits of scan based logic BIST
- Fast test-per-clock operation
  - > 2 orders of magnitude faster
- Improved fault coverage
- Rich two and multi-pattern delay tests
Conceptual Schematic for Classical Scan

Data In → $L_1$ (Clkph1) → MUX (0 → 1) → $L_3$ (Clkph2) → Data Out

Scan In → $L_2$ (Clkph1) → Test Control C

Scan Out
Conceptual Schematic for Classical Scan

Normal functional operation (C=0)
Conceptual Schematic for Classical Scan

Scan shift operation (C=1)
Multi-Mode Scan Memory Element
Multi-Mode Scan Memory Element

Data In → L1 → 0 MUX → L3 → Data Out

Scan In → L2 → 0 MUX → L4 → Scan Out

Test Control C

Normal Operation/Scan Shift (C=0)
Psuedorandom Self-Test (C=1)

Multi-Mode Scan Memory Element

Diagram showing the flow of data with inputs and outputs labeled as follows:
- Data In
- Data Out
- Scan In
- Scan Out
- Test Control C

The diagram illustrates the flow of data through various components labeled L1, L2, MUX, L3, and L4.
Normal Operation/Scan Shift Mode
Normal Operation/Scan Shift Mode

Independent Scan Register
- SCAN/MISA Register
Normal Operation/Scan Shift Mode

Note: No switching activity in the scan chain if Scan-In is held steady at 0 (or 1)
Pseudorandom Self-Test Mode

- Scan/MISA Register provides state input
- Next state vector is accumulated (modulo 2) in (shifted) Scan/MISA Register
- Rich random patterns in Scan/MISA Register
Pseudorandom Self-Test Mode

- Test-per-clock operation in self-test mode
- Random patterns in Scan/MISA Register provide rich 2-pattern and multi pattern tests
- Actual functional paths tested for timing delays
Register Adjacency

Fig. 7. State Dependencies in (a) CSTP and (b) MME Designs
Timing Tests

- Two sequential test vector inputs $<V_1 V_2>$ cause a change at an output.
- The switching delay is the time from the application (launch) of $V_2$ until change at the output.
Scan Based Delay Testing

Launch-on-Shift

LOGIC

Data In

MUX

Flip Flop

Data Out

Scan In

Scan Enable

Clock

V1

V2

Clock Edge 1: Launch V2 (scan = 1)

Then switch scan = 0

Clock Edge 2: Capture response to V1>V2 change in Flip Flop

Figure 3. A simplified timing diagram of a launch-from-shift transition delay fault (TDF) pattern.
Launch-on-Capture

Clock Edge 1: Apply V1 (scan = 1)
Then switch scan = 0

Clock Edge 2: Capture response to V1 in Flip Flop to launch timed transition. This is V2

Clock Edge 3: Capture response to V2

Figure 4. Simplified timing diagram of a launch-from-capture (broadside) TDF pattern.

LOGIC

Scan Based Delay Testing

Data In

V2 =

Data Out

Response[V1]

UX

M

Flip Flop

Clock

Scan In

Scan Enable
Simulation Results for Transition Delay Fault Coverage

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<th>Curve under test</th>
<th>Indep vectors</th>
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Implementation Issues

- MME has identical pin-outs as standard scan
- Approx 50% larger cell area
- Comparable performance (lower output loading)
Implementation Issues

- Clock controlled standard scan less effective for delay testing
- Scan clock must be guard-banded for skews relative to clock phase 2
Conclusions

- Multi-Mode Scan provides test-per-clock self-test
- Rich mix or random vectors to support delay testing of true functional paths
- Minimal need for test access to core: IEEE 1149.1
- Supports traditional scan for diagnosis
- Ease of design: identical cell pin-outs as traditional scan
Open Problems

- Handling large number of X-states
- Covering random pattern resistive faults
- Delay Testing
  - MMSCAN can efficiently support FMAX testing
Fmax Testing

• Fmax Testing finds the highest clock rate for which a circuit passes a given (TDF) test set
• A binary search using repeated applications of the test set is performed to obtain Fmax
• An abnormal Fmax value compared to other circuits from the lot indicates a defect that may cause a functional or reliability failure in the field
Fmax for TDF pattern for 32 parts that pass dc tests but fail system level tests [1]
Fmax Testing

- Fmax outliers may experience a delay failure in the field because delay test sets often cannot test worst case signal propagation conditions.

- Fmax outliers may also contain latent defects that can cause early life failure.
Questions?