VLSI Power Estimation & Dual-Transition Glitch Filtering in Probabilistic Simulation

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Outline

- **Introduction**
  - Levels of power estimation techniques

- **Gate-level Probabilistic Approach**
  - Signal Probability
  - Transition probability
  - Transition density
  - Probability waveform

- **Dual-transition glitch filtering**
  - Idea and examples
  - Detailed algorithm
  - Experimental results

- **Summary**
Introduction

- Power estimation is critical to IC (low power) design
  - Total power consumption must be estimated during the design phase.
  - Helps identifying hot-spot on the chip, useful for thermal design
- Levels of power estimation
  - Transistor Level
  - Gate Level
  - RTL Level
  - Behavior Level
  - Software Level
- Two approaches
  - Simulation based
  - Non-simulative
Simulation based approach

- Transistor Level Simulation
  - Circuit level
    - SPICE
      - Solving a large matrix of node current using KCL
      - Components - Resistor, capacitor, inductors, current sources and voltage sources.
      - Diodes and transistors are modeled by basic components
    - PowerMill
      - Table based device model
      - Event driven timing simulation
      - 2-3 orders of magnitude faster than Spice
Simulation based approach

- **Switch level**
  - Transistor as a on-off switch with a resistor
  - Short circuit power - observing the time in which the switches form a power-ground path

- **Gate Level Simulation**
  - Components - logic gates
  - Logic simulation to find switching activity, \( P = \frac{1}{2}CV^2f_{\text{active}} \)
  - Monte Carlo simulation, statistical method
    - Each sample has \( N \) Random input vector
    - Energy consumption has a normal distribution
    - Stopping criterion derived from sample average and sample standard deviation
Simulation based approach

- RTL level simulation
  - Components - register, adder, multiplier, etc.
  - Macro-modeling of each component based on simulation
    - Simulating the component with random input
    - Fitting a multi-variable regression curve (power macro model equation) using a least mean square error fit.
  - RT-level simulation collect input statistics of each module
High level estimation

- Behavior level estimation
  - No much information about gate level structure of design component
  - Information theoretic models
    - Average switching activity for each line is approximated by $\frac{1}{2}$ its entropy
    - Total capacitance estimated based on output entropy
  - Complexity based models, “equivalent gate”

- Software level estimation
  - Energy consumption by a application program
  - Instruction level power macro-modeling
  - Profile-driven program synthesis with RT level simulation
Non-simulative approach

- Gate level probabilistic approach
  - Concepts
    - Signal Probability
    - Transition probability
    - Transition density
    - Probability waveform
  - Factors in building up a model
    - Spatial, temporal correlation
    - Zero delay or real delay (glitch power)
    - With or w/o glitch filtering
Gate level probabilistic approach - concepts

○ Signal Probability
  ● $P_s(x)$, the fraction of clock cycles in which the steady-state value of signal $x$ is high
  ● Spatial independence, the logic value of an input node is independent of the logic value of other input nodes
  ● Under spatial independence
    ○ Inverter: $c=a$, $P_s(c)=1-P_s(a)$
    ○ AND gate: $c=ab$, $P_s(c)=P_s(a)P_s(b)$
    ○ OR gate: $c=a+b$, $P_s(c)=1-[1-P_s(a)][1-P_s(b)]$

○ Signal correlation
  ● $P_s(x_1,x_2)=P_s(x_1)P_s(x_2)W_{x_1,x_2}$
Signal probability with spatial correlation

- **Global OBDD**
  - Ordered binary decision diagram corresponding to the global function of a node (function of node in terms of circuit input)
  - Give exact signal correlation
  - Example, function $y = x_1x_2 + x_1x_3$

$P_s(y) = P_s(x_1)P_s(f_{x_1}) + P_s(x_1)P_s(f_{x_1})$

- Traversal from bottom to top to derive signal probability
Gate level probabilistic approach - concepts

- Transition probability
  - $P_t(x)$, average fraction of clock cycles in which the steady state value of $x$ is different from its initial value
  - Temporal independence, the signal value of a node at current clock cycle is independent to its signal value at previous clock cycles
  - Under temporal independence assumption
    - $P_t(x) = 2P_s(x)[1 - P_s(x)]$

- Transition correlation
  - Zero delay assumption, lag one markov chain
    - $TC_{xy}(ij,mn) = P(x_{i->j},y_{m->n}) / P(x_{i->j})P(y_{m->n})$ where $i,j,m,n \in \{0,1\}$
Gate level probabilistic approach - concepts

○ Transition density
  ● $D(x)$, average number of transitions a logic signal $x$ makes in a unit time (one clock cycle)
  ● Boolean difference, if $y$ is a function depending on $x$ then
    \[ \frac{\partial y}{\partial x} = y|_{x=1} \oplus y|_{x=0} \]
    
    and
    \[ D(y) = \sum_{i=1}^{n} P(\frac{\partial y}{\partial x_i})D(x_i) \]
  ● Assume no two signal transit simultaneously.
  ● Assume spatial independence
  ● Glitch power included w/o glitch filtering effect
Gate level probabilistic approach - concepts

- Probabilistic simulation
  - Probability waveform, a sequence of signal probability and transition probability over signal transition interval
  - Real delay model, spatial independence
  - Transition density, sum of transition probabilities
  - Our refined definitions
    - **Signal probability** $s_{p_n}(t)$, probability of node $n$ having logic 1 at time $t$
    - **Transition probability** $P^s_{n}(t)$, probability that node $n$ has a logic transition state $s$ ($s \in \{00, 01, 10, 11\}$) at time $t$
    - Properties: $s_{p_n}(t-) = P^{10}_{n}(t) + P^{11}_{n}(t)$, $s_{p_n}(t+) = P^{01}_{n}(t) + P^{11}_{n}(t)$
Probability waveform

- An example
Probability waveform propagation

○ AND gate, $c=ab$

\[ P_{c}^{01}(t_{1}) = P_{a}^{01}(t_{1})P_{b}^{01}(t_{1}) + P_{a}^{01}(t_{1})P_{b}^{11}(t_{1}) + P_{a}^{11}(t_{1})P_{b}^{01}(t_{1}) \]
\[ = 0.1 \times 0.1 + 0.1 \times 0.3 + 0.3 \times 0.1 \]
\[ = 0.07 \]

\[ P_{c}^{10}(t_{1}) = P_{a}^{10}(t_{1})P_{b}^{10}(t_{1}) + P_{a}^{10}(t_{1})P_{b}^{11}(t_{1}) + P_{a}^{11}(t_{1})P_{b}^{10}(t_{1}) \]
\[ = 0.2 \times 0.2 + 0.2 \times 0.3 + 0.3 \times 0.2 \]
\[ = 0.16 \]

\[ P_{c}^{11}(t_{1}) = sp_{c}(t_{1}+) - P_{c}^{10}(t_{1})+ = 0.25 - 0.16 = 0.09 \]

\[ sp_{c}(t_{1}+) = P_{c}^{01}(t_{1}) + P_{c}^{11}(t_{1}) = 0.07 + 0.09 = 0.16 \]
Tagged Probabilistic Simulation

- Partition of probability waveform according to the steady state signal values, \( w^{00}_{n}, w^{01}_{n}, w^{10}_{n}, w^{11}_{n} \)
- Approximate exact spatial correlations with the macroscopic spatial correlations between steady state signal values (tags)

\[
\omega_{a,b}^{xy,wz} = \frac{P(w^{xy}_{a} \land w^{wz}_{b})}{P(w^{xy}_{a})P(w^{wz}_{b})}
\]

- Glitch filtering effect attempted
Tagged probability waveform

○ Definitions
  ● Signal probability, $sp_{n,xy}^n(t)$, probability of node $n$ having logic 1 at time $t$ on waveform $w_{n,xy}^n$. $x,y \in \{0,1\}$
  ● Transition probability, $Ps_{n,xy}^n(t)$, probability that node $n$ has a logic transition state $s$ ($s \in \{00,01,10,11\}$) at time $t$ on waveform $w_{n,xy}^n$

○ Propagation of waveform
  ● Similar to untagged waveform
    ○ Two input gates, 16 joint tagged waveform combined to 4 output waveform
  ● For an two inputs AND gate, $c=ab$

\[
P_{c,(xy,wz)}^{01}(t+d) = (P_{a,xy}^{01}(t)P_{b,wz}^{11}(t) + P_{a,xy}^{01}(t)P_{b,wz}^{01}(t) + P_{a,xy}^{11}(t)P_{b,wz}^{01}(t))\omega_{xy,wz}
\]

\[
P_{c,(xy,wz)}^{10}(t+d) = (P_{a,xy}^{10}(t)P_{b,wz}^{11}(t) + P_{a,xy}^{10}(t)P_{b,wz}^{10}(t) + P_{a,xy}^{11}(t)P_{b,wz}^{10}(t))\omega_{xy,wz}
\]

where $x,y,w,z \in \{0,1\}$
New glitch filtering method

- Original glitch filtering scheme in TPS
  - If pulse width less than gate inertial delay $d$, it is subject to glitch filtering
  - Example, two input AND gate for time $t1$ for all $t2$, where $t2-t1<d$
    \[
    p_{01}^{c,(xy,wz)}(t1+d) = p_{01}^{a,xy}(t1) p_{10}^{b,wz}(t2) \omega_{a,b}^{xy,wz} \\
    p_{10}^{c,(xy,wz)}(t2+d) = p_{01}^{a,xy}(t1) p_{10}^{b,wz}(t2) \omega_{a,b}^{xy,wz}
    \]
- Limitations
  - Imprecise, not an accurate description of glitch
  - Can’t filter glitch coming from single input
Original glitch filtering in TPS

\[ t_1 < t_2 < t_3 < t_1 + d \]

Actual waveform

TPS Glitch filtering
New glitch filtering method

- Dual-transition probability
  - Find the exact condition for a pulse, knowing that each signal has 4 possible state at t1, t2
  - In probability waveform

\[
P_{01,10}(t_1,t_2) = P\{c \text{ is } 0 \rightarrow 1 \text{ at } t_1 \text{ and } 1 \rightarrow 0 \text{ at } t_2\}
\]

\[
= P\{(a,b) \text{ at } t_1 \text{ is } (01,11) \text{ or } (11,01) \text{ or } (01,01) \text{ and } (a,b) \text{ at } t_2 \text{ is } (10,11) \text{ or } (11,10) \text{ or } (10,10)\}
\]
Dual-transition probability

- $P_{01,10}^{c}(t_1,t_2)$ is a sum of 9 product terms
  - Example term: $P_{01,10}^{a}(t_1,t_2)P_{11,11}^{b}(t_1,t_2)$
Dual-transition probability

- In TPS, use macroscopic spatial correlations to approximate spatial correlations

\[ P_{c,(xy,wz)}^{01,10}(t_1 + d, t_2 + d) = \sum_{i=1}^{3} \sum_{j=1}^{3} P_{a,xy}^{sa_i,sa_j}(t_1, t_2) P_{b,wz}^{sb_i,sb_j}(t_1, t_2) \omega_{a,b}^{xy,wz} \]

\[(sa_i, sb_i) \in \{(01,11), (11,01), (01,01)\}\]

\[(sa_j, sb_j) \in \{(10,11), (11,10), (10,10)\}\]

\[x, y, w, z \in \{0,1\}\]
New glitch filtering method

- Dual-transition glitch filtering
  - If pulse width less than gate inertial delay $d$, it is subject to glitch filtering
  - For a two input AND gate for time $t_1$
    for all $t_2$, where $t_2-t_1<d$

$$p_{01}^{c,(xy,wz)}(t_1) = p_{01,10}^{c,(xy,wz)}(t_1,t_2)$$
$$p_{10}^{c,(xy,wz)}(t_2) = p_{01,10}^{c,(xy,wz)}(t_1,t_2)$$

$$p_{10}^{c,(xy,wz)}(t_1) = p_{10,01}^{c,(xy,wz)}(t_1,t_2)$$
$$p_{01}^{c,(xy,wz)}(t_2) = p_{10,01}^{c,(xy,wz)}(t_1,t_2)$$
Dual-transition glitch filtering

t_1 < t_2 < t_3 < t_1 + d

\[
P_{c,11}^{10,01}(t_i', t_{i'}') = 0.2 \times 0.3 + 0... + 0 = 0.06
\]

\[
P_{c,11}^{10,01}(t_2', t_3') = 0.2 \times 0.3 + 0... + 0 = 0.06
\]

\[
P_{c,11}^{10,01}(t_1', t_3') = 0.2 \times 0.2 + 0... + 0 = 0.04
\]
Dual-transition probability propagation

- **Dual-transition probability**
  - Propagated from primary inputs towards output
  - General equation
    \[
    P_{sc_1,sc_2}^{x,y,w}(t_1 + d, t_2 + d) = \sum_{i=1}^{k} \sum_{j=1}^{l} P_{sa_1,sa_2}^{x,y}(t_1, t_2) P_{sb_1,sb_2}^{x,y}(t_1, t_2) \omega_{a,b}^{x,y,wz}
    \]
  - For primary inputs, transition only occur at time 0
    - \( P_{sn_1,sn_2}^{x,y}(0, t) = P_{sn_1}^{x,y}(0) \) if \( sn_1, sn_2 \) is a valid sequence of state,
      - e.g. \( P_{11}^{01,11}(0, t) = P_{11}^{01}(0) \)
    - Otherwise, \( P_{sn_1,sn_2}^{x,y}(0, t) = 0 \)
Update dual-transition probability

- No two transition can occur within gate delay \( d \) after the filtering.
- Dual-transition correlation coefficient
  \[
  \omega_{n,xy}^{sn1,sn2}(t_1,t_2) = \frac{P_{n,xy}^{sn1,sn2}(t_1,t_2)}{P_{n,xy}^{sn1}(t_1)P_{n,xy}^{sn2}(t_2)}
  \]

- After the filtering
  - If \( t_2-t_1<d \),
    - \( P_{n,xy}^{01,10}(t1,t2) \), \( P_{n,xy}^{10,01}(t1,t2) \) set to 0
    - \( P_{n,xy}^{01,11}(t1,t2) \) set to \( P_{n,xy}^{01}(t1) \) ....
  - Otherwise
    - Update
      \[
      P_{n,xy}^{sn1,sn2}(t_1,t_2) = P_{n,xy}^{sn1}(t_1)P_{n,xy}^{sn2}(t_2)\omega_{n,xy}^{sn1,sn2}(t_1,t_2)
      \]
      where \( P_{n,xy}^{sn1}(t1) \), \( P_{n,xy}^{sn2}(t2) \) are transition probability after the filtering.
Experimental results

- Dual-transition glitch filtering is implemented in both probabilistic simulation and TPS
  - ProSim+DT
  - TPS+DT
- Stand alone software implemented in C++
  - Input - circuit netlist, signal probabilities
  - Output – power (transition density) for each node and the total power
- Results compared to event driven logic simulation
  - Assuming spatial and temporal independence for primary inputs
  - 40,000 randomly generated vectors
- Steady state signal probability and macroscopic correlations are obtained from a zero delay simulator
Experimental results

- Small tree structure circuit
  - No spatial correlations
  - Arbitrarily specified delay
  - Input signal probability = 0.5
  - $P_{\text{switching}}$, switching power in terms of transition density $D_x$
Experimental results – tree circuit

<table>
<thead>
<tr>
<th>Nd</th>
<th>Logic Sim.</th>
<th>ProSim</th>
<th>ProSim+DT</th>
<th>TPS</th>
<th>TPS+DT</th>
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<tbody>
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<td>$P_{\text{switch}}$ ($D_x$)</td>
<td>$P_{\text{switch}}$ ($D_x$)</td>
<td>Err. (%)</td>
<td>$P_{\text{switch}}$ ($D_x$)</td>
<td>Err. (%)</td>
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</table>
Experimental results – tree circuit

- Observations
  - ProSim gives large error because it neglects glitch filtering at nodes 26, 28, 30, 31
  - Original TPS gives large error at node 30, 31 because of inaccurate glitch filtering
  - For tree structure circuit, ProSim+DT and TPS+DT has similar accuracy because there is no spatial correlations
Experimental results – benchmark circuits

- ISCAS 85’ benchmark circuits
- Input signal probability 0.5
- Gate delay is proportional to number of fanouts
- Error statistics
  - $E_{\text{avg}}$, average node error, percentage error with respect to average node power obtained from logic simulation
  - $\sigma$, standard deviation of node errors
  - $E_{\text{tot}}$, percentage error of total power
- Results from ProSim+DT, TPS, TPS+DT are compared with logic simulation results
### Experimental results – benchmark circuits

<table>
<thead>
<tr>
<th>Circuits</th>
<th>ProSim+DT</th>
<th>TPS</th>
<th>TPS+DT</th>
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<tbody>
<tr>
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<td>$E_{\text{avg}}$ (%)</td>
<td>$\sigma$(%)</td>
<td>$E_{\text{tot}}$ (%)</td>
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<td>6.6</td>
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<td>Max.</td>
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Experimental results – benchmark circuits

- **Observations**
  - ProSim+DT gives large error because it neglects spatial correlations
  - TPS+DT has up to 29% improvement on $E_{tot}$
    - c432, c1355, c6288 contains a large component of glitch power
    - Estimation accuracy is improved due to the new glitch filtering method
  - TPS+DT gives a more consistent estimation in terms of average and maximum errors
  - TPS+DT gives larger error for certain circuits
    - Estimation accuracy is jointly decided by TPS and DT
    - Effectiveness of DT is limited by the inherent errors in TPS
Experimental results – computation cost

- TPS+DT is 2-3 times faster than the logic simulation over all input vectors.
- ProSim+DT is 20-30 times faster than the logic simulation.
- Original TPS is 2 order of magnitude faster than logic simulation.
- TPS+DT is much slower due to the propagation of dual-transition probabilities.
- ProSim+DT is faster since it only has one probability waveform for each node.
  - Idea for tree structure circuit where no spatial correlation exists.
Summary

- Intro. to different Levels of power estimation
- Gate-level Probabilistic Approach
  - Signal Probability, Transition probability, Transition density
  - Probabilistic simulation, tagged probabilistic simulation
- A improved glitch filtering method
  - A new concept of dual-transition probability
  - Can be applied to both probabilistic simulation and Tagged probabilistic simulation
  - Enhanced TPS achieves a more accurate and consistent estimation, with up to 29% improvement on estimation accuracy
  - Accuracy and computation cost needs to be improved
## Recent works

- Some more improvements on estimation accuracy is obtained

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<th>Circuits</th>
<th>TPS</th>
<th>TPS+DT</th>
<th>New method</th>
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Questions?

For questions and comments, please contact me at 
href="hufeih01@auburn.edu"