We wish to add 512 Kbytes of external static RAM (SRAM) and 128 Mbytes of external flash memory (FLASH) to our microcontroller system, interfaced to the processor via the Flexible Static Memory Controller (FSMC) on the STM32F407 microcontroller.

The following companies manufacture memory devices that will enable us to add the desired memory with one SRAM chip and two FLASH chips.

**Integrated Device Technology** (www.idt.com)
The IDT 71V416 SRAM chip contains 512 Kbytes of static RAM.

**Micron** (www.micron.com)
The Micron JS28F512P33BFD chip contains 64 Mbytes of parallel NOR flash memory.

For the SRAM chip, find its data sheet on the manufacturer’s web site and use it (plus the course slides) to answer the following questions.

1. What is the external “organization” of the memory? (ex. N Kbytes x M bits)
2. List the address and data pins on the chip that correspond to the information in the previous question, and describe how the organization can be derived by looking only at these pins.
3. What block of addresses should the chip be assigned within the Cortex-M address space? (Hint: This is dependent on the FSMC NOR/PSRAM enable bit to be connected to the memory’s chip-enable input.) The range should be written as: \[ start-address \ldots end-address \], with addresses written in hexadecimal.
4. What power supply voltage(s) are required for the chip?
5. What is the read access time of the chip?
6. Sketch a block diagram, or provide a list, showing how each SRAM pin should be connected to the appropriate FSMC pin. To save time, show data and address pins collectively as Dn-Dk or An-Ak, where n and k are bit numbers. Control signals should be shown individually. You do not need to show power supply and ground pins for this step.
7. Discuss how you would modify address line connections to add a second SRAM chip in the address range immediately following that of the first chip.

Repeat the above for the FLASH chip(s).