Final Exam: Graduate Course – VLSI Testing
Auburn Univ., ELEC 7250, Spring 2005

April 30, 2005

Instructions (please read before you proceed):
1. Please read all problems before starting your answers. Problems can be answered in any order.
2. Attempt all five problems and attempt all parts within each problem.
3. Answers can be written on question sheets or separate sheets or a combination. Each sheet should have a page number and problem number. On the first sheet write your name and the total number of sheets you are submitting.
4. Before handing in your answers, please check them thoroughly. If necessary, extra 10 minutes can be allowed for checking.

Problem 1: Fault Modeling (20 Points)

(a) In a single-output circuit if two faults are indistinguishable, i.e., they produce the same output function, then prove that the faults have the same set of tests. (10 points)

(b) For the circuit of Figure 1, derive tests for faults i sa1 and e sa0. (5 points)

\[
\begin{array}{c}
\text{a} \\
\text{b} \\
\text{c} \\
\text{f} \\
\text{e} \\
\text{d} \\
\text{g} \\
\text{h} \\
\text{i} \\
\text{j} \\
\text{k} \\
\text{l} \\
\text{m} \\
\text{sum} \\
\text{carry}
\end{array}
\]

Figure 1: Circuit for Problem 1 on fault modeling.

(c) Are two faults in part (b) distinguishable? If yes, how will you distinguish between them? If not, why not? (5 points)
Solution to Problem 1

(a) Consider a Boolean vector $X$, a logic function $f(X)$, and two faults with corresponding functions $f_1(X)$ and $f_2(X)$. For the faults to be indistinguishable, the two faulty functions must assume identical values for all $X$:

$$f_1(X) \equiv f_2(X), \forall X \tag{1}$$

Assume that vector $X_1$ is a test for fault 1. Then,

$$f_1(X_1) \oplus f(X_1) = 1 \tag{2}$$

From Equation (1) $f_1(X_1) \equiv f_2(X_1)$ and substituting this in Equation (2) we get

$$f_2(X_1) \oplus f(X_1) = 1 \tag{3}$$

which implies that $X_1$ is also a test for fault 2. Similarly, any test $X_2$ for fault 2 can be shown to be a test for fault 1. Thus, both faults have exactly the same tests.

(b) Both faults, $i\text{ sa1}$ and $e\text{ sa0}$, are detected by exactly one vector, $a = b = 1$. This vector is simulated for both faults in parallel in the following figure.

Parallel fault simulation of test $a = b = 1$ for circuit of Figure 1.

(c) Even though the two faults have the same test set, they are distinguishable because the two faulty functions differ at each output. For the faults to be indistinguishable, the condition of Equation (1) in part (a) must be satisfied at each output. The following table gives a diagnostic procedure:
Problem 2: Testability Measures (20 Points)

(a) For the asynchronous circuit of Figure 2 compute SCOAP combinational controllability ($CC_0, CC_1$) and combinational observability ($CO$) measures for all lines. (10 points)

(b) Assuming that the testability of a fault can be represented as the sum of the appropriate controllability and observability (e.g., testability measure of a stuck-at-1 fault will be $CC_0 + CO$), identify the most difficult to test stuck-at fault. (5 points)

(c) Derive a test for the fault identified in part (b), considering line $j$ to be in unknown state, initially. (5 points)

Solution to Problem 2

(a) Combinational SCOAP testability measures, $CC_0$, $CC_1$ and $CO$, are shown in the following figure. Initially, line $j$ is set to $CC_0 = CC_1 = CO = \infty$. All values stabilize after two iterations.

(b) The highest testability measure is $CC_0 + CO = 6 + 6 = 12$ for fault $j$ sa1.

(c) A test for the fault $j$ sa1 consists of two vectors, $(a, b) = (0, 1) \rightarrow (X, 0)$. Derivation of this test by time-frame expansion is illustrated in the following

\[
\begin{array}{|c|c|c|c|c|}
\hline
\text{Inputs} & \text{Outputs} & \text{Fault} \\
\text{a} & \text{b} & \text{sum} & \text{carry} & \text{diagnosis} \\
\hline
1 & 1 & 0 & 1 & \text{No fault} \\
1 & 1 & 1 & 1 & \text{Fault i sa1 is present} \\
1 & 1 & 0 & 0 & \text{Fault e sa0 is present} \\
1 & 1 & 1 & 0 & \text{Some other fault is present} \\
\hline
\end{array}
\]
SCOAP measures, \((CC0, CC1) CO\), for the circuit of Figure 2.

Asynchronous feedback from \(h\) to \(j\) is broken and initialization \(j = X\) is used. The stability of signals in each time-frame is verified by applying the new state of \(h\) into \(j\).

Test generation for fault \(j\) sa1 in the circuit of Figure 2.
Problem 3: ATPG and fault simulation (20 Points)

Derive a pseudo-combinational circuit for the cycle-free sequential circuit of Figure 3 by shorting all flip-flops (FF). Obtain a combinational test for the fault \( g \) sa1 in the pseudo-combinational circuit. If you succeed in finding a combinational vector then using fault simulation of the sequential circuit show that the targeted fault is detected by repeating the same vector. Otherwise, use the time-frame expansion method to derive a test sequence for this fault. (20 points)

![Figure 3: Circuit for Problem 3.](image)

Solution to Problem 3

The pseudo-combinational circuit for the circuit of Figure 3 is shown below:

![Pseudo-combinational circuit for sequential circuit of Figure 3.](image)

A test for \( g \) sa1 in the pseudo-combinational circuit is impossible because \( a = b = 0 \) input that is essential to activate the fault, blocks the observation of the fault effect through the NAND gate \( j \).

This fault is testable in the sequential circuit of Figure 3 because the activation of the fault and propagation through \( j \) can take place in separate time-frames. A valid test consists of four vectors, \((a, b) = (X,0), (0,1), (X,1), (1,X)\). Its derivation is shown in the following figure:
Problem 4: Fault diagnosis (20 points)

A circuit has six faults that are tested by four tests. Table 1 shows the fault dictionary, where $t_i = 1$ for fault $F_j$ if $i$th test detects $F_j$. Faults $F_1$ and $F_5$ occur with negligible probability and all other faults are found to be equally likely in a faulty circuit. Devise a diagnostic tree to minimize the average time of diagnosing a faulty circuit. Given a faulty circuit, on an average how many tests will be applied before the fault is found. (20 points)

Table 1: Fault dictionary for Problem 4.

<table>
<thead>
<tr>
<th>Fault</th>
<th>Occurrence probability</th>
<th>Test syndrome $t_i$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>$t_1$ $t_2$ $t_3$ $t_4$</td>
</tr>
<tr>
<td>No fault</td>
<td>-</td>
<td>0 0 0 0</td>
</tr>
<tr>
<td>$F_1$</td>
<td>0.00</td>
<td>0 0 0 1</td>
</tr>
<tr>
<td>$F_2$</td>
<td>0.25</td>
<td>1 0 0 0</td>
</tr>
<tr>
<td>$F_3$</td>
<td>0.25</td>
<td>0 0 1 0</td>
</tr>
<tr>
<td>$F_4$</td>
<td>0.25</td>
<td>0 1 0 0</td>
</tr>
<tr>
<td>$F_5$</td>
<td>0.00</td>
<td>1 0 1 0</td>
</tr>
<tr>
<td>$F_6$</td>
<td>0.25</td>
<td>0 1 0 1</td>
</tr>
</tbody>
</table>

Test generation for $g\text{ sa1}$ fault in the sequential circuit of Figure 3.
Solution to Problem 4

Let us denote the tests as $T_1$, $T_2$, $T_3$ and $T_4$, such that $t_i$ is the test syndrome of $T_i$. We will only consider the four faults that have non-zero probabilities of occurrence. A binary search generally leads to an optimum diagnosis since each test provides a pass/fail result. Examining the tests of Table 1, we find that application of $T_2$ divides the fault set into subsets $(F_4, F_6)$ and $(F_2, F_3)$. Similar consideration leads to the following diagnostic tree. We have assumed that the circuit is known to be faulty before the diagnosis begins. Time for diagnosis is estimated as follows:

$$\text{Average diagnostic test length} = 2 \times \text{Prob}(F_4) + 2 \times \text{Prob}(F_6) + 2 \times \text{Prob}(F_2) + 2 \times \text{Prob}(F_3)$$

$$= 2 \times 0.25 + 2 \times 0.25 + 2 \times 0.25 + 2 \times 0.25$$

$$= 2.0$$

The average diagnosis time is two times that of applying one test.
Problem 5: Scan Design (20 Points)

The circuit in Figure 4 is a sequence detector. Only one 100-bit long sequence 0...11010 in the input bit-stream at PI produces an output PO = 1. The 100-input AND function is implemented as a tree network of AND gates. The circuit is customized for a specific bit-stream by inverting the selected inputs of the AND network.

![Figure 4: Circuit for scan design Problem 5.](image)

(a) Considering the AND function as a stand-alone combinational circuit, what is the minimum number of combinational vectors to completely test all single stuck-at faults? (5 points)

(b) Implement scan design with minimum hardware and test pin overheads. What is the test length in clock cycles for testing the combinational logic and the shift register? (10 points)

(c) Modify the design to reduce the test time by a factor of 10. Add minimal hardware and no more than 20 pins to the original circuit. (5 points)

Solution to Problem 5

(a) The AND gate will require 101 combinational vectors:

- A single all-1 vector will detect all 100 s-a-0 faults.
- A single s-a-1 fault on an input line i will be tested by a vector containing i = 0 and all other inputs set to 1. Since there are 100 such faults, 100 vectors will be needed.
- Inverters on input line will require the corresponding bit of the vector to be complemented. Because of the equivalence of their input and output faults, inverters do not require any additional tests.
- Tests for input stuck-at faults will cover all other faults in the AND tree. This is according to the checkpoint theorem on fault dominance.

(b) The minimal scan design requires only one extra pin that is used as the scanout signal that is necessary for testing the shift register. PI would be used as
scanin. Because scanin and scanout are always available, no test control signal is required. The circuit is shown in the following figure:

Minimum overhead scan design of the circuit of Figure 4.
Only one pin for scan-out is added.

The shift register test will require \( N_{FF} + 4 = 104 \) clock cycles. For combinational tests of the AND gate, as soon as a vector is scanned in, the output of the AND gate is directly observed. So, no scan-out is needed. Thus, application of 101 combinational vectors will take \( 101 \times 100 = 10,100 \) clocks. The total length of the scan test is \( 104 + 10,100 = 10,204 \) clock cycles.

(c) To reduce the test time, nine scan multiplexers are inserted to break up the shift register into 10 segments, each containing 10 flip-flops. All multiplexers are controlled by a test control signal TC. The PI signal is used as the scan-in signal, scanin-1, for the first shift register segment. The other nine segments are supplied the scan-in through test pins, scanin-2 through scanin-10. Each shift register segment has a test output pin. The scan schematic is shown in the following figure:

Reduced test time scan design of the circuit of Figure 4.
Hardware overhead is shown as grey shaded area.

The scan overhead consists of nine multiplexers and 20 pins (TC, 9 scanins, and 10 scanouts).
All shift register segments are tested in parallel by a sequence of 14 clocks. Scanning in of each combinational vector takes 10 clocks and, therefore, 1,010 clocks will be needed to apply 101 vectors. Thus, total test time is $14 + 1,010 = 1,024$ clock cycles.