Figure 9.34: RAM system organization.

Method:

1. Zero out memory.
2. Increase the power supply above \( V_{CC} \) in steps of 0.01 V. For each voltage setting, read the memory. Stop as soon as a 1 is read from any location, and record this supply voltage as \( V_{\text{high}} \).
3. Fill the memory with 1s.
4. Slowly decrease the supply below \( V_{CC} \) in steps of 0.01 V. For each setting, read the memory. Stop as soon as a 0 is read from any location, and record this supply voltage as \( V_{\text{low}} \).

Possible test outcomes:

1. \( V_{\text{high}} \) and \( V_{\text{low}} \) are inconsistent with data book values (fails.)

DC parametric tests are simple and inexpensive, and measure worst case loading. They are inadequate as functional or timing tests, and only test a few devices connected to the terminals, leaving the rest of the chip untested.

Leakage Test. This finds the worst case input leakage current (input leakage) or tristated output leakage current (tristated leakage.)