Non-Intrusive BIST - Organization

- Architecture Implementations
  - Board-level
  - Device-level
  - System-level
  - Vertical Testability
- Benefits and Limitations
Non-Intrusive BIST

- Architectures avoid manipulation of internal CUT circuitry
  - BIST circuitry is external to CUT
  - Low performance penalty
    - Good for high speed applications
Board-Level Implementations

- Programmable logic devices (FPGAs & CPLDs) are excellent devices for board-level BIST
  - Reprogram with BIST circuitry for testing
  - Reprogram for system function during operation
    - No area overhead or performance penalty
    - Must store configuration data to reprogram PLD
- Provide TPG, MISR, & BIST control for board-level STUMPS
Device-Level Implementations

- TPG & MISR can be shared
- Loopback mechanism needed
- Good for data path circuitry
  - Control circuitry tested via multiple test sessions

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(a) simplex data path
(b) duplex data path with loopback
Bit-Sliced BIST Circuit Design

- One bit-slice per bit in data path
- Additional XOR gates for LFSR polynomial
- Optional flip-flops for pipelining high speed applications

<table>
<thead>
<tr>
<th>$B_0$</th>
<th>$B_1$</th>
<th>Function</th>
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<tr>
<td></td>
<td>0 0</td>
<td>Hold</td>
</tr>
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<td>0 1</td>
<td>LFSR</td>
</tr>
<tr>
<td></td>
<td>1 0</td>
<td>D flip-flop</td>
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<tr>
<td></td>
<td>1 1</td>
<td>MISR</td>
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System-Level Implementation & Testing

- PCB Inputs
  - ![Diagram showing system layout]

(a) **board-level testing**
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(b) **device-level testing**
Non-Intrusive BIST
(c) **interconnect testing**

*denotes loopback activated*
Non-Intrusive BIST Summary

**Benefits**
- Low area overhead
- Low performance penalty
  - Good for high speed applications
- Vertical testability for device through system-level testing

**Limitations**
- Low fault coverage for many applications
  - Fault simulation may be lengthy
    - But necessary to determine fault coverage