Write a VHDL model for an \( N \)-bit, rising edge-triggered, internal feedback Linear Feedback Shift Register (LFSR) with programmable characteristic polynomial (POLY) and an active high synchronous preset (PRE). The outputs of the LFSR are the \( N \)-outputs (LFSR). Use a default value of \( N=4 \) and verify that the polynomial \( X^4+X^3+1 \) is a primitive polynomial. Use the following I/O ordering and naming: ins: CLK, PRE, POLY, outs: LFSR. The model must be capable of re-sizing by only changing the generic default value for \( N \) (and no other lines of VHDL code); you can verify this with the 5-bit primitive polynomial \( X^5+X^2+1 \).

Simulate, debug, and verify your model using Mentor Graphics (see the links to Dr. Nelson’s Mentor Graphics tutorials on the class web page). Turn in a print out of your VHDL model and your simulation results for your working model. The assignment is due at the beginning of class, Tuesday, October 19.