ELEC 6740 Electronics Manufacturing
Chapter 7: Design for Manufacturability, Testing & Repair

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Outline

- DFM Organizational Structure
- General Design Considerations
- Component Selection Considerations for Manufacturability
- Soldering Considerations
- Interpackage Spacing Considerations
- Via Hole Considerations
- Soldermask Considerations
- Repairability Considerations
- Cleanliness Considerations
- Testability Considerations
Sequential design vs. concurrent engineering

- Physical layout
  - Manufacturing
    - Test
      - Design
  - Design
- Logic design
- Manufacturing
- Test
- Process engineers
- Design
- Reliability engineers
- Product engineers
General Design Considerations

- **Standard form factor (board size, shape, tooling holes)**
  - Odd shapes can require special fixtures, etc.
  - **Standard assembly panel size vs. board size**
    - Optimization of boards per assembly panel
    - Optimization of assembly panels per PWB panel
    - \( L/W \leq 1.5 \)
Scoring of Panels
Fiducials or Alignment Marks

BGA Alignment marks

Target Position for BGA (shaded area): Center alignment mark

Global Fiducial Placement
- Any three corners
- 0.180 clearance area free of traces, solder mask, legend, labels, holes, board edge, etc.

Local Fiducial Placement for fine pitch
- At the center or at the corner
- 0.180 clearance area free of traces, solder mask, legend, labels, holes, board edge, etc.
Fiducials or Alignment Marks

Note: Solid round dot typically 0.060 inch diameter preferred

Shapes other than circle for fiducials
- Solid square typically 0.080 inch on a side
- Solid diamond typically 0.080 inch on a side
- Single cross hair typically 0.080 inch high
- Double cross hair typically 0.080 inch high
Component Selection

- Use surface mount components that solve real estate constraints or reduce the number of manufacturing steps and bear no cost premium.

- All surface mount components should be autoplaceable
  - Tantalum caps with welded studs
  - Connectors
  - Heat sinks
  - Sockets
Component Selection

- Components terminations with solder plating are better than solder dipped
- Select only components that can withstand the reflow temperatures
- Use 1206 and 0805 components when possible, 0603, 0402 & 0201 components are harder to place
- Use X7R capacitors rather than Z5U when using wave soldering to avoid cracking
Component Selection

- Do not wave solder capacitors larger than 1812 to avoid cracking
- Do not use ceramic parts larger than 0.250” on FR-4 to avoid CTE mismatch and potential reliability concerns
- Use marked components if no cost premium
- For secondary side attachment in Type II or Type III SMT use low profile SOT devices instead of high profile SOTs. Low profile are easier for adhesive attachment, but high profile are easier to clean
Component Selection

- Avoid using MELF packages unless very cost driven (MELF package cheaper)
- Use Nickel barrier terminated capacitors and resistors to prevent leaching of termination into molten solder
- Avoid surface mount connectors & sockets without over riding reasons
Component Selection

- Use qualified parts
- Minimize the different types of components
Soldering Considerations
Soldering Considerations

- Options
  - Double sided reflow + hand soldering
  - Reflow side 1 & wave solder side 2
    - May degrade reliability of side 2 SMT components during wave soldering
    - Flux can creep into SOIC and PLCC packages
  - Double sided reflow with DIP using butt joints
    - Reliability of butt joint
    - Not permitted for military and high reliability applications
  - Double sided reflow with ‘paste-in-hole’
  - Reflow side 1 & wave solder side 2 with shield
Wave Solder Shield

Cover plate for overall bottom side surface mount devices
Solder Shield

- **Stainless Steel or Titanium**
  - Titanium expensive & hard to machine but holds shape better for repeated use
- **Aluminum or copper shield contaminates solder pot**
- **High temperature plastics and composites are also used**
Savings by Converting SMT
No Savings by Converting

Solder Paste

Chip Components

PLCC
Chip Component
SO
DIP
Other Soldering Considerations

- Place larger components on top (2nd) reflow side when using double sided reflow.
- Wave solder is not cheaper than reflow so wave solder can be considered if only SMT passives on 1 side.
- Wave solder fills plated through holes allowing vacuum to hold board down for automated test.
Component Orientation

- Uneven fillets

- Solder skips can occur on trailing termination

Figure 7.9 Uneven fillets or solder skips will result if both component terminations are not soldered simultaneously.
Component Orientation

* When pad-to-pad dimension is less than .100, smaller component must enter wave first, because of shadowing

Figure 7.10  Recommended component orientation for wave soldering.
Component Orientation

Figure 7.11 Minimum distance between staggered components to prevent shadowing of trailing component in wave soldering.
Component Orientation

Preferred IC orientation

Robber pads will reduce solder bridging

Figure 7.12 Preferred SOIC orientation with “robber pads” on the trailing sides.
Figure 7.13 Poor and good layout patterns of SOICs for wave soldering. Use only one package type in a given row.
Component Orientation

As viewed from the secondary side
- Location of chip/through hole components to reduce defects.
- None within SOIC Row
- OK on trailing or leading edges

Figure 7.14 Acceptable and unacceptable locations of through-hole pins in SOIC rows for wave soldering.
Interpackage Spacing

- Use land patterns described in Chapter 6
- For mixed assemblies, autoinsert equipment requires about 0.100” clearance for through hole devices
- About 0.075 to 0.085” clearance is needed for automated and hand probe testing
- The interpackage spacing must allow for test probe at ATE.
Interpackage Spacing

- Automated cleaning with adequate pressure nozzles (>30psi)
- Component shift during reflow soldering and placement may be up to 25% of the pad width for military and 50% for commercial applications
- Solder joint melting of adjacent components is allowed a total of 4 times (2 for assembly and 2 for rework)
- Visual inspection (board tilting)
Interpackage Spacing

Figure 7.15  Minimum pad-to-pad clearances between surface mount pads of active devices for reflow soldering. At least 100 mils of clearance must be provided all around the fine pitch land patterns to allow multi-level paste printing. (See Figure 9.21 in Chapter 9.)
Figure 7.16 Minimum pad-to-pad clearances between surface mount pads of active devices for reflow soldering and through-hole devices for wave soldering.
Interpackage Spacing

Figure 7.17  Minimum pad-to-pad clearances between surface mount pads of passive devices and DIPs for wave soldering.
Interpackage Spacing

Figure 7.18 Minimum pad-to-pad clearances for a surface mount and through-hole PGA and axial component for wave soldering.
# Interpackage Spacing

Table 7.1  A summary of MINIMUM interpackage spacings among various types of surface mount and through-hole components.

<table>
<thead>
<tr>
<th></th>
<th>MINIMUM SPACING (MILS)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>PLCC/SOJ</td>
</tr>
<tr>
<td></td>
<td>PAD, SIDE</td>
</tr>
<tr>
<td></td>
<td>SO/R-PACK PAD, SIDE</td>
</tr>
<tr>
<td></td>
<td>SO/SOJ/R-PACK BODY, END</td>
</tr>
<tr>
<td></td>
<td>CHIP COMPONENT PAD, SIDE</td>
</tr>
<tr>
<td></td>
<td>CHIP COMPONENT PAD, END</td>
</tr>
<tr>
<td>PLCC/SOJ side, pad to</td>
<td>60°</td>
</tr>
<tr>
<td>SO/R-Pack side, pad to</td>
<td>60°</td>
</tr>
<tr>
<td>SO/SOJ/R-pack end, body to</td>
<td>70°</td>
</tr>
<tr>
<td>Chip component side, pad to</td>
<td>70°</td>
</tr>
<tr>
<td>Chip component end, pad to</td>
<td>40</td>
</tr>
<tr>
<td>DIP side, pad to</td>
<td>60</td>
</tr>
<tr>
<td>DIP end, body to</td>
<td>70°</td>
</tr>
<tr>
<td>Axial side, body to</td>
<td>70°</td>
</tr>
<tr>
<td>Axial end, pad to</td>
<td>60</td>
</tr>
<tr>
<td>Stake pin, pad to</td>
<td>70°</td>
</tr>
<tr>
<td>Other component, body to</td>
<td>70°</td>
</tr>
</tbody>
</table>

*°A 10 mils smaller gap may be used between components in a memory array.

NOTE: Allow at least 100 mils of clearance all around the land pattern of a fine pitch (under 25 mil pitch) device.
Via Holes

- Number decreased with switch to SMT, but did not go away
- SMT vias are smaller than Through Holes for components
- Vias are used for test probe contact
- Vias must be filled (solder or solder mask) for vacuum used in bed-of-nails ATE.
- Vias should not be used in SMT pads
- Via hole location a concern in reflow due to limited solder volume, but not in wave solder
# Via Holes

Table 7.2  Via hole and plated through-hole comparisons in an Intel single-sided computer board before and after its conversion to SMT.

<table>
<thead>
<tr>
<th></th>
<th>THROUGH-HOLE MOUNT VERSION</th>
<th>SURFACE MOUNT VERSION</th>
</tr>
</thead>
<tbody>
<tr>
<td>Component holes</td>
<td>3150</td>
<td>1300</td>
</tr>
<tr>
<td>Via holes</td>
<td>800</td>
<td>2200</td>
</tr>
<tr>
<td>Total holes</td>
<td>3950</td>
<td>3500</td>
</tr>
</tbody>
</table>
Via Holes

Figure 7.19 Good design practice for via hole location in surface mount boards.
Via Holes

Figure 7.20   Poor design for reflow soldering.
Tented Vias

Figure 7.21  Tented via hole with solder mask.
Tented Vias

- **Dry film**
  - Should not be used between pads of chip components
  - 0.003-0.004” thick can lead to tombstoning
  - Thinner dry film can be used
  - Allows tenting
Tented Vias

- **Wet film**
  - Thinner, allows traces to be run between pads of passive components
  - Vias must be plugged before tenting
  - Increases adhesive bond strength, and minimizes voids during adhesive cure
Solder Mask

- **Solder mask should not be used over Sn/Pb**
  - Solder melts during reflow causing solder mask to crack
  - Entrapping flux and moisture

- **SMOBC – solder mask over bare copper**
Repairability

- Hand repair
- Automated systems with hot air
- Maximum of 2 rework cycles to limit Sn-Cu intermetallic formation
Repairability

Figure 7.22  Equipment for the repair of passive devices: (left) conductive and (right) hot air with mechanical tweezers.
Repairability

Figure 7.23 Chip capacitor under SOJ package used in memory modules.
Testing

- In through hole technology, all leads are accessible on the bottom side of the board.
- With SMT, test points must be provided for ‘in-circuit’ test.
  - Test point take up space.
  - No test point, no in-circuit test.
- Functional vs. In-circuit.
ATE

- Use 1 test point (TP) for ground and 1 TP for power for every 10 ICs to reduce risk of ringing.
- Connect all unused pins to ground or power via a resistor to improve quality of test.
- Whenever possible, avoid double sided test probe approach to reduce fixturing and cost.
- One TP is needed for every test node unless 100% capability is needed for individual components.
ATE

- Test point spacings should be 0.100” whenever possible. Probes for smaller spacings are fragile and prone to damage.
- For smaller TPs (under 30 mils dia.) deposit solder paste on the TPs to form bumps for ease of probing with serrated test probes.
- Flux residue can interfere with probe contact.
Figure 7.24 Interpackage spacing for ATE testing for 50 and 100 mil test probes.