**Miniaturized Data Acquisition System for Extreme Temperature Environments**

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Abstract—A data acquisition system is being developed for use on the NASA Lunar-Mars series of missions. The unit will accept inputs from multiple types of sensors, employing three types of input channels that each incorporate programmable elements to accommodate a wider variety of input signals. Based in part on a subsystem called the Remote Health Node (RHN) that was originally developed during the 1990s for use on the now-defunct NASA X-33 "space plane", the Remote Electronics Unit (REU) is being developed using a 0.5 micron Silicon Germanium (SiGe) BiCMOS technology from IBM with a circuit library that has been designed to operate normally across a temperature range from -180 degrees C up through +125 degrees C.

The REU will support sixteen input channels, including twelve low speed channels designed for signals in the 1-200 Hz range, two higher speed channels that support inputs up to 5 KHz, and two charge amplifier channels that support piezoelectric transducers up to 5 KHz. All sixteen input channels reside on a single mixed signal ASIC that includes analog-to-digital (A/D) conversion to provide a digital output for back-end processing of the signals. The low speed and high speed channels incorporate a programmable Wheatstone bridge that can be programmed as a 3/4, 1/2, or full bridge, along with variable gain amplifiers. The A/D converter employs a novel Wilkinson architecture that allows 16 inputs without the use of an analog multiplexer, employs common circuitry to minimize die area, and dissipates very little power.

The programmable elements of the input channels are controlled by a Field Programmable Gate Array (FPGA) that also provides signals for both sensor stimulation and input channel calibration. These signals are translated to analog values by a pair of digital-to-analog (D/A) converters that reside on each of the low and high speed channels. The stimulus is boosted to higher voltages through use of a current mirror that employs special high voltage transistors that do not require any special processing steps. Back-end processing will also include a small processor to supply commands and accept data before passing the information on to the main computer via RS-485 links.

Support of extreme temperatures is achieved through the use of device models that have been extended to cover the desired temperature range, adapted technology ground rules to support long term reliability, and unique packages that are designed for this extended range. The circuitry employs both heterojunction bipolar transistors (HBTs) and field effect transistors (FETs). Where needed, radiation hardened by design (RHBD) techniques are being employed in the circuits to provide mitigation against single event latch-up (SEL), single event upsets (SEU), and total dose accumulation.

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1. INTRODUCTION

Operation of robotic planetary rovers on the lunar and Mars surface exposes these vehicles to an extreme set of temperatures. During the period when the rover is exposed to full sun, temperatures may reach or even exceed +120 degrees centigrade. However, when the rover is in the dark and within a lunar crater where it is shielded from all sunlight, the ambient temperature may fall to roughly -180 degrees centigrade in the equatorial regions, similar to that of liquid nitrogen. Within shadows of polar craters, temperatures can drop even further to -230 degrees C. As a result, all of the electronics of the rover vehicle are carefully contained within a heater box to maintain their lower end temperatures to within the MIL-STD-883 specification of -55 degrees centigrade. This results in two key problems. First, the power required to maintain the heater box itself detracts from the total available power, constraining the possible scientific capabilities of the rover. Second, the need to place all of the electronics centrally results in a mass of wiring between the box and elements at the extremities such as the cameras, robotic arm, and wheels. This set of wires both increases mass and decreases reliability of the rover.

This problem is replicated on the surface of spaceborne satellites and manned vehicles. Clearly, the need existed to develop a set of versatile electronics to support the extreme range of temperatures found in these applications. NASA headquarters is funding a team consisting of Universities and commercial contractors to address this problem as part of the Exploration Technology Development Program (ETDP).

The team is developing a library of reusable circuit elements using the IBM 0.5 micron Silicon Germanium (SiGe) BiCMOS technology, with process models extended for the region between -55 degrees C and -180 degrees C. These circuits can be assembled either discretely or into larger ASICs to create a variety of functional units that address mission-specific needs, and additional circuits can be added to further extend the application space. A large library of mixed signal circuits has already been designed, manufactured, and tested across the temperature range. Radiation hardened by design (RHBD) techniques are being employed to reliable spaceborne operation. Manufacturing is being coordinated through MOSIS as part of multi-project wafer runs.

The first application chosen to demonstrate the value of this technology is a Remote Electronics Unit (REU) which is designed to collect data from a variety of sensors that can be located outside a spacecraft or external to the heater box found on planetary vehicles. The design is partially based on the Remote Health Node (RHN) box originally developed by BAE Systems in the late 1990s that employed discrete components and hybrid packaging technology.

This paper discusses the Remote Health node and the approach that is being employed to migrate key functions of this unit into monolithic SiGe BiCMOS ASICs. The incremental development approach is discussed, along with ongoing plans for development and insertion into NASA programs. This effort is funded as part of NASA’s Exploration Technology Development Program, under contracts NNL05AA37C and NNL06AA29C “Silicon-Germanium Integrated Electronics for Extreme Environments”.

2. THE REMOTE HEALTH NODE

The Remote Health Node (RHN) box, upon which the REU is being based, was developed for the X-33 reusable launch vehicle (RLV) as an element of the vehicle health management system during the late 1990s [1]. The RHN boxes were designed to be distributed around the periphery of the spacecraft in proximity to the sensors themselves, with over 50 units to be deployed on each X-33. As shown in Figure 1, the RHNs communicated with the vehicle health management computer via a Fiber Distributed Data Interface (FDDI) optical bus in a dual token ring topology. The RHN, as shown in Figure 2, was programmable to support a variety of sensors that included accelerometers, strain gauges, thermocouples, Resistive Temperature Devices (RTD), pressure (individual and 64 channel pressure scanner), rate (RPM and flow meters), synchro-resolver (angle), voltage, current, angular rate, and linear position. Several different types of input channels were created to support this large range of devices.
transducers, thermocouples, using power. Various gauges. Twenty accelerometers and similar devices were also four charge amplifier channels for interface to piezoelectric transducers, and single channels of various other types.

Figure 2: Block Diagram of the Remote Health Node

Twenty four low speed channels accepted inputs such as thermocouples, resistive temperature devices, and strain gauges. Four higher rate channels accepted inputs from accelerometers and similar sensors. There were also four charge amplifier channels for interface to piezoelectric transducers, and single channels of various other types.

Figure 3: Remote Health Node for X-33

The RHN box shown in Figure 3 measured 3” by 5” by 6.75”, weighed 11 kilograms, and dissipated 17 Watts of power. Connectors on one end interfaced to the sensors. Optical fiber connectors were located on the opposite side of the box.

The mixed signal portion of the RHN consisted of the various input channels, an A/D converter to translate the analog sensor data, and D/A converters to drive stimulus signals. The microcontroller was PowerPC-based with an associated FPGA to interface to the analog front end. To optimize packaging, the RHN elements were assembled using circuit boards connected using flex connectors [2].

3. THE REU ARCHITECTURE

The Remote Electronics Unit (REU) will reproduce the majority of function currently found in the RHN box in a smaller form factor with lower weight and dissipating less power, with electronics that are radiation hardened and support an extreme temperature range. As envisioned, the entire REU would fit within one of the connectors used to interface to the sixteen sensors it will support. A pair of connectors similar to the one being considered for the REU is shown on the right side of the existing RHN box in Figure 3. As in the case of the RHN box upon which it is modeled, the REU will continue to interface to a larger computer for data analysis and processing, although the dual fiber optic bus interface will be replaced.

The planned REU will include a front-end mixed-signal ASIC that incorporates multiple channels of three types: low speed channels for sensors at rates below 200 Hz, high speed channels for sensors with rates up to 5 KHz, and charge amplifier channels for piezoelectric transducers. The mixed-signal ASIC will be supported by a digital function based on an 8031 architecture microcontroller with an RS-485 bus interface for communication with the main system computer. An FPGA function that provides the control and data interfaces to the mixed signal ASIC will also be included, similar to that found in the original RHN but adapted to support the unique implementation of the channels on the mixed signal ASIC. Full integration of the digital functions into a second ASIC is one possible implementation, although other options are also being considered. Multi-chip module packaging is being developed that would provide the maximum level of integration to minimize weight, volume, and power dissipation.

The high levels of monolithic integration will significantly reduce REU size, weight, and power dissipation when compared to the original RHN. Decrease in volume is projected to approach a level where the REU size is driven primarily by the size of the connectors required for sensor interface. Component matching is inherently improved as well. Inherent limitations of this approach are supply voltage limitations associated with the target 0.5 micron SiGe BiCMOS technology and current handling constraints that prevent integration of power FETs. Where the original RHN box accepted +28 Volt power, the REU is powered by a 3.3 Volt supply.
As shown in Figure 4, it is possible to expose the entire REU to the extreme temperature ambient environment, eliminating the large mass of sensor interface wiring that it typically required to route sensor outputs to the electronics located within a “heater box” or similar temperature controlled environment. In this example, the main system computer which is represented by BAE Systems’ RAD750™ radiation hardened processor continues to require temperature control, but connections across that boundary are now limited to the serial interfaces coming from the REUs. Some of the sensors used with the original RHN are also shown in the figure as examples of sensor inputs that could be used with the REU.

4. THE REU MIXED-SIGNAL ASIC

The REU mixed-signal ASIC will include sixteen input channels, including twelve low performance channels, two high performance channels, and two charge amplifier channels that interface to piezoelectric transducers. Both the low speed and high speed channels include integrated programmable Wheatstone bridge circuits. They accommodate a wide variety of sensors by allowing configuration in order to complete full, half, or quarter bridge sensors through internal switch settings. The channels come together into a 16-channel A/D converter. Integrated D/A converters are used for both stimulus and channel calibration, and unique high voltage transistors are employed to provide drive at voltage levels higher than those typically supported by the target BiCMOS technology to external power FETs that provide stimulus to the sensors as required.

Like the original RHN channels, the REU low speed channels are designed for input signals up to 200 Hz, while the high performance channels and charge amplifier channels support input signals as high as 5 KHz. These higher speed channels both include Butterworth filters to provide sharp cutoff of the high frequencies.

The programmable Wheatstone bridge is configured through the use of solid state NMOS pass transistor-based single pole single throw (SPST) switches in series with the resistor legs of the bridge. The resistors and switches have been designed and laid out as an integrated embeddable circuit element. These are programmed from the digital control logic and stored in shift registers that reside within the mixed-signal ASIC that are loaded serially to minimize ASIC pin count. The shift registers are initialized to values appropriate for each application, but their contents are considered static for the mission duration.

The 16-channel 12-bit A/D converter employs the Wilkinson architecture to reduce power dissipation and minimal die area. The Wilkinson architecture allows replication of only part of each channel such as the auto-zero comparator while employing common circuitry for the ramp generator and counter. The counter operates at speeds much higher than the A/D converter sampling rate, reflecting 4,096 states counted per sample. As such, while the A/D converter is designed to sample at a maximum rate of 20 kSPS to guarantee 4x oversampling of the high speed 5 KHz signals, the counter operates at 80 MHz.

The block diagram of the integrated ASIC is shown in Figure 5. Five-wire interfaces on both the high
performance and low performance channels combine signals and stimulus lines. Two of the three possible signal inputs are used in each case, reflecting the Wheatstone bridge variation used for each individual channel. Serial shift registers are used to load configuration information for gain, bridge configuration, and stimulus current into the channels. This ASIC, estimated as 10mm by 12mm in size, is scheduled for tape out in February 2008 and will be processed by the IBM foundry through a MOSIS multi-project wafer release.

![Diagram of the ASIC](image)

**Figure 5: Functional Block Diagram of the REU Mixed Signal ASIC**

The output of the ASIC is a 6-bit digital output from the 12-bit A/D converter. The choice to transfer 6 bits at a time was made to minimize pin count and power dissipation. The high bits vs. low bits are selected by a signal fed from the digital control logic on the companion ASIC. Scan strings have also been provided in the ASIC for test purposes, selected by a test mode signal pin and separated from the serial shift that is employed during functional initialization of the REU. The test scan strings are limited in length to less than 100 flip-flops apiece for test efficiency.

5. **Incremental Integration Methodology**

The development of the mixed-signal ASIC is following a methodology in which incremental progress is made in the design and integration of the key elements of the design. At the most basic level, individual circuits are developed with a plan of reuse in the larger ASIC and for later programs. These circuits are placed on individual test chips with integrated bonding pads and assembled into larger “tiles” for manufacturing. Datasheets are generated to provide documentation of the design, including the concept of operation, electrical and physical characteristics, and physical design about both the test chip and the reusable core function.

A system of configuration management has been defined to allow individual circuit developers to release stable versions of their designs to the chip integrators, while maintaining working level files separately. One member of each University circuit design team has been designated the coordinator for configuration management. This team member controls the upload of design data into the configuration managed database hosted by Lynguent. Standard naming conventions for circuits and net names have also been documented to allow integrators to identify signals requiring global connections.

Once the circuit has been validated in hardware, it can be incorporated into higher levels of integration. In the case of the mixed signal ASIC, the very first level of monolithic integration involved the development of a partial low speed channel, a release dubbed “CRYO-2.5” in reference to the program phase. The block diagram of the full low speed channel is shown in Figure 6, with the partial channel implementation partitioned out for documentation purposes. This partial channel was released to manufacturing in May 2007 and is currently in hardware testing.

The partial channel was interfaced to an integrated temperature sensor to provide a stimulus for early testing. A second channel was also included on the tile with sensor inputs that were brought out to package pins for connection to an external sensor. An FPGA was developed to provide the control signals for the A/D converter for test purposes. The functions in this FPGA will be integrated with other digital control functions such as the channel configuration and gain control logic in the final REU implementation.

At that same time, individual circuits for the D/A converters, shift registers, and other circuits were released. Both the partially integrated channel and the individual circuits were assembled into a 5mm by 6mm “tile”.

The fully integrated low speed channel was released to manufacturing on September 24, 2007, along with examples of the high speed channel and charge amplifier channel in a release called “CRYO-3a”. Also released at that time were a number of individual circuits, including matching circuits with and without radiation hardened by design enhancements for comparative testing. Circuits that were incorporated into the channels that either had not been previously hardware validated or had been modified based on hardware test results were included individually as well to allow isolated testing. The September 2007 release consisted of three 5mm by 6mm tiles, one for the example channels and two others for circuits and experiments.
Hardware of the three-channel version of the ASIC was received at the beginning of December 2007. Once packaged, the individual channels will be tested by accessing the analog outputs that feed the A/D converter inputs. Following that, the three channel ASIC will be tested with the integrated 16-input A/D converter. A screen shot of the tile containing the three prototype channels and the 16-input A/D converter is shown in Figure 7. The basic low speed channel whose block diagram is displayed in Figure 6 is located in the upper left hand corner of the die. The more complex and higher performance channel that also includes the Wheatstone bridge is located in the upper right hand corner. The charge amplifier channel is on the lower right side of the die, and the A/D converter occupies the center and lower left side. At the far lower left hand corner of the die are two copies of the high voltage current source circuit that will be used to drive sensor stimulus through an external power FET in both the low and high speed channels in the final design.

Figure 7: Extreme Temperature Electronics Three Channel Tile

Simultaneously, a methodology for simulation of these highly integrated mixed signal designs was being defined.
The approach involves use of combined behavioral and circuit level models, and basic examples have already been coded and demonstrated. A goal for the next release is to perform simulations of each individual channel, followed by a full simulation of the multiple channel ASIC. In addition to locally-based simulation platforms, access to a cluster of machines at the Georgia Institute of Technology has been provided for team members. This will allow faster turnaround of iterations across temperature, voltage, and process corners.

Regular coordination and review teleconferences were held that included the use of web-based collaboration software that allowed each student designer to discuss the method and progress of each individual development effort. This approach is important in bringing together the large group of professors and students from several Universities as well as the industry members into a more cohesive team with a common, focused goal.

6. REU Digital Control Functions

The REU has a digital control section in addition to the mixed-signal front end. The original RHN digital functions consisted of a PowerPC microcontroller, a programmable FPGA that could be programmed either for built-in unit test or for functional operation, both volatile and non-volatile memory, and the FDDI optical interface.

The digital control within the REU will be implemented in a simpler manner, driven in part by the modest semiconductor technology used in this program. A small microprocessor based on the Intel 8031 architecture [3] that is being developed by a related project in the same process technology, will provide basic commands.

Ideally, the interface logic to the analog circuitry will continue to be programmable, based on either an external FPGA or through use of an embedded FPGA function. An early sizing of the original FPGA design from the RHN box indicated that implementation of the code in an embedded FPGA core was a viable alternative to reproduce this functionality even given the modest process technology. If the goal of implementing the channel control circuitry with field programmable logic cannot be achieved, use of the asynchronous standard cell library developed for the microprocessor program is an alternative approach that may be employed. Because of differences in the analog front-end implementation, the FPGA function will require some level of redesign before it can be employed in the REU.

Some limited amount of on-chip SRAM will be provided, estimated as two blocks of 4 KB by extrapolating from the size of the 128 word by 8 bit memory array developed for the 8031 processor. The interface to a larger computer will be handled by RS-485 transceivers that have already been designed and hardware validated. Additional memory capacity, both volatile and non-volatile, may be required externally.

Both the processor circuits [4] and the FPGA test circuits [5, 6] are based on asynchronous "clockless" logic that allows timing to skew as needed. The processor circuitry employs the use of hysteresis and the FPGA is based on a handshakeing architecture. This approach minimizes the adverse effect on path timing vs. clock distribution across the extremely wide temperature range that the REU will be expected to operate across. The SRAM will be based on the memory designed for use inside the 8031 processor. That basic memory circuitry (SRAM array cells and matching peripheral control circuitry) was developed in modular function to allow reassembly into a variety of shapes and sizes.

![Functional Block Diagram of the REU Digital Control ASIC](image)

Figure 8: Functional Block Diagram of the REU Digital Control ASIC

Elements of all three of these circuits were released to manufacturing as part of the September 2007 MOSIS multi-project wafer. The FPGA test circuits, developed by researchers at Cornell University, were one of the many small experiments and individual circuits that were released on the 5mm by 6mm tiles by the NASA-funded team. Key sub-elements of the microprocessor including the SRAM macro were released on a separate tile by the University of Arkansas as part of its own program.

A functional block diagram of the REU digital control ASIC is shown in Figure 8. In the current plan, this ASIC will be released to manufacturing in mid-2008.

7. Underlying Technologies

The REU would not be possible without the key lower level semiconductor and packaging technologies that have been extended for use in extreme temperature environments. The
SiGe BiCMOS technology originally developed by IBM for mixed-signal commercial designs exhibits excellent performance characteristics across a wide temperature range if specific groundrule limitations are observed while designing the circuits.

This 0.5 micron technology which is designated “5AM” is also relatively low in cost, a function of the very conservative lithography in current terms that lowers masks costs and can be processed with less expensive tooling. Several variations of the technology were investigated and compared early in the project as analog circuits were being developed and tested [7]. However, these variants were determined to be unnecessary, allowing manufacturing with an essentially standard BiCMOS process. Wafers for use across the extreme temperature range are being produced with a back-side metal, the only modification required of the process.

The SiGe process and the heterojunction bipolar transistors being used within the circuits also demonstrate inherently high tolerance to Total Ionizing Dose (TID) radiation, and that the effects of irradiation at low temperatures (77 degrees Kelvin) are less severe than at room temperature for the 0.5 micron technology [8, 9]. The CMOS n-type MOSFETs that are also part of the process are less inherently resistant to TID irradiation. As a result, radiation hardened by design (RHBD) techniques are being employed to overcome these issues [10] as well as to address sensitivities to Single Event Effects (SEE). For example, guard rings are being added to the circuits to protect against latch-up. Comparative examples of circuits both with and without RHBD enhancements were released to manufacturing in September 2007 as part of the same multi-project wafer as that used for the three channel tile.

Once the base technology was characterized across the full temperature range, the team developed a transistor model for the extreme cold temperature range. This model is used in conjunction with the existing commercial transistor model to provide simulation capability throughout the temperature range. Attempts to generate a single transistor model that covered the entire temperature range remain an active area of investigation.

Unique packaging technology has also been developed by the team for extreme temperature operation. A unique combination of alloys and materials is employed to support the mechanical stresses associated with such a large variation in temperature due to different coefficients of thermal expansion. Both wire bond and “flip-chip” packages are being developed, based on Aluminum Nitride (AlN) and Silicon Nitride (Si₃N₄) substrates, respectively and Aluminum Oxide (Al₂O₃) ceramic packages [11]. Focus is on multi-chip modules to reduce the levels and associated weight of packaging. Interconnection of die is being achieved with a multilayer copper and polyamide structure.

8. INSERTION PLANS

The existing RHBD boxes are already being used in a test laboratory at Marshall Space Flight Center in Huntsville, Alabama. This facility is experimenting with technologies for the next generation of manned missions to the lunar surface. Early versions of the SiGe extreme temperature REU chips will be provided to this team for insertion and eventual replacement and use in platforms such as the Crew Exploration Vehicle, Crew Launch Vehicle, Lunar Lander, and others.

An early flight insertion of the example channel is released in September 2007 on the CRYO-3a tile is being considered by Boeing for a Materials International Space Station Experiment (MISSE) on the MISSE-7, planned for launch in late 2008. Control for the channels will be provided by an Actel fuse-based FPGA. The goal of the MISSE missions is to characterize the performance of new materials to the space environment.

9. SUMMARY

Supported by NASA funding and the Georgia Electronic Design Center at Georgia Tech, a team comprised of both university and corporate members is developing a Remote Electronics Unit for use in space missions where the electronics will be exposed to extreme temperature environments. Based in concept on the Remote Health Node box developed in the 1990s by BAE Systems, the REU will decrease size, weight, and power dissipation while simultaneously increasing resistance to radiation and extending operation to extreme temperatures. The REU components are being manufactured in a 0.5 micron BiCMOS technology and an incremental integration approach is being employed for ASIC development. The goal of the program is to provide a REU capable of NASA mission insertion by the conclusion of the program in 2009.

The achievements described here would not have been possible without the efforts of a large number of graduate students and co-workers. While too numerous to list, their work and dedication has been and will continue to be greatly appreciated. We are grateful for the support of C. Moore, M. Watson, A. Keys, M. Beatty, L. Nadeau of NASA, E. Kolawa of JPL, and the IBM SiGe development group.
REFERENCES


BIographies

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John D. Cressler received the B.S. degree in physics from the Georgia Institute of Technology (Georgia Tech), Atlanta, GA in 1984, and the M.S. and Ph.D. degrees in applied physics from Columbia University, New York, in 1987 and 1990, respectively. From 1984 to 1992 he was on the research staff at the IBM Thomas J. Watson Research Center in Yorktown Heights, NY, and from 1992 to 2002 on the faculty at Auburn University, Auburn, AL. In 2002, he joined the faculty at Georgia Tech, where he is currently Ken Byers Professor of electrical and computer engineering. His research interests include: Si-based (SiGe/strained-Si) heterostructure devices and technology, mixed-signal circuits built from these devices, radiation effects, cryogenic electronics, device-to-circuit interactions, noise and reliability physics, device-level simulation, and compact circuit modeling. Dr. Cressler has published over 350 papers related to his research. He is the co-author (with Guofu Niu) of "Silicon-Germanium Heterojunction Bipolar Transistors", Artech House, Boston, MA, 2003, author of "Reinventing Teenagers: the Gentle Art of Instilling Character in Our Young People", Xlibris, Philadelphia, PA, 2004, and editor of "Silicon Heterostructure Handbook: Materials, Fabrication, Devices, Circuits, and Applications of SiGe and Si Strained-Layer Epitaxy", CRC Press, Boca Raton, FL, 2006.


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Fa Foster Dai (M'92–SM'00) received a Ph.D. degree in electrical and computer engineering from Auburn University, AL, in 1997 and another Ph.D. degree in electrical engineering from The Pennsylvania State University, PA, in 1998.

From 1997 to 2000, he was with Hughes Network Systems, Germantown, Maryland, where he was a Member of Technical Staff in VLSI, designing analog and digital ICs for wireless and satellite communications. From 2000 to 2001, he was with YAFO Networks, Hanover, Maryland, where he was a Technical Manager, leading high-speed IC designs for fiber communications. From 2001 to 2002, he was with Cognito Inc., Gaithersburg, Maryland, designing RFICs for integrated multi-band MIMO wireless transceivers. From 2002 to 2004, he was a consultant for Cognito Inc. In August 2002, he joined the faculty of Auburn University in Alabama, USA, where he is currently a professor in electrical and computer engineering. His research interests include VLSI circuits, RFIC designs for wireless and broadband communications, ultra-high frequency synthesis and analog/mixed-signal built-in self-test (BIST). He is the co-author of “Integrated Circuit Design for High-Speed Frequency Synthesis” (Artech House Publishers, Feb. 2006).

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Jim Holmes joined Lynguent after 13 years at Texas Instruments, where he was an analog/mixed-signal system-on-chip (SoCs) modeling and simulation specialist. While there he focused on validation and verification of over 40 SoCs, spanning consumer applications from servo control in hard disk drives to baseband processing in cellular phones. He supported AMS modeling activities worldwide at Texas Instruments' design centers, as well as its customer and contractor sites. He developed key modeling methods that unified specification, design, and test activities across the globe. In 2004, Holmes was elected Senior Member Technical Staff at Texas Instruments. Jim currently leads Lynguent's research team that is commercializing an expert system for analog/mixed-signal model composition and analysis. He holds a BS and an MS in Electrical Engineering from the University of Connecticut.
Dr. Mohammad Mojarradi is an expert in developing mixed-signal/mixed-voltage electronic circuits for drive and control of actuators, power supplies, sensors and micro-machined electromechanical interface applications. He manages the development of the electronic circuits for the “thermal cycle resistant electronics” task for Mars Science Laboratory at JPL and leads a research consortium of universities developing electronics for extreme environments. He received his Ph.D from UCLA in 1986, has twenty-five patents, eighty publications and is a senior member of IEEE. Prior to joining JPL, he was an Associate Professor at Washington State University and the Manager of the mixed-voltage/specialty integrated circuit group at the Xerox Microelectronics Center, El Segundo, CA.

Patrick McCluskey is an Associate Professor of Mechanical Engineering at the University of Maryland, College Park where he is associated with the CALCE Electronic Products and Systems Center. He has published extensively in the area of packaging and reliability of electronics and microsystems for high power and extreme temperature environments, including two books and numerous book chapters. He has also served as general or technical chairman for numerous conferences in these research areas. Dr. McCluskey is an associate editor of the IEEE Transactions on Components and Packaging Technologies. He received his Ph.D, in Materials Science and Engineering from Lehigh University.

Benjamin J. Blalock received his B.S. degree in electrical engineering from The University of Tennessee, Knoxville, in 1991 and the M.S. and Ph.D. degrees, also in electrical engineering, from the Georgia Institute of Technology, Atlanta, in 1993 and 1996 respectively. He is currently an Associate Professor in the Department of Electrical Engineering and Computer Science at The University of Tennessee where he directs the Integrated Circuits and Systems Laboratory (ICASL). His research focus there includes analog integrated circuit design for extreme environments (both wide temperature and radiation) on CMOS and SiGe BiCMOS, multi-gate transistors and circuits on SOI, analog circuit techniques for sub 100-nm CMOS, mixed-signal/mixed-voltage circuit design for systems-on-a-chip, and biomicroelectronics. Dr. Blalock has co-authored over 80 refereed papers. He has also worked as an analog IC design consultant. Dr. Blalock is a senior member of the IEEE.

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