A 9-bit Quadrature Direct Digital Synthesizer Implemented in 0.18-μm SiGe BiCMOS Technology

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Abstract—This paper describes a 9-bit 6.2-GHz low power quadrature direct digital synthesizer (DDS) implemented in a 0.18-μm SiGe BiCMOS technology. With a 9-bit pipeline accumulator and two 8-bit sine-weighted current steering DACs, this DDS is capable of generating quadrature sinusoidal waveforms up to 3.15 GHz with a maximum clock frequency of 6.2 GHz. Packed with more than 13,500 transistors, the quadrature DDS occupies an active area of 2.3 × 2.5 mm² and a total die area of 3.0 × 3.0 mm². The measured spurious-free dynamic range is approximately 26 dBc at a clock frequency 6.2 GHz. At the maximum clock frequency, the power consumption of the DDS is 2.5 W with 3.3- and 4.0-V power supplies for the digital and analog parts, respectively. The DDS thus achieves a power efficiency figure-of-merit of 5.04 GHz/W/phase. The DDS chips were packaged with 48-pin ceramic leadless chip carriers and air cooling was used during the measurement.

Index Terms—Direct digital synthesizer (DDS), frequency synthesizers, silicon germanium (SiGe), waveform generators.

I. INTRODUCTION

A D AR SYSTEMS demand highly accurate control over the output frequencies and phases of the frequency synthesizers in the radar transceiver for coherent detection. It is not uncommon that the modern radar systems require frequency synthesizers with low power consumption, high output frequency, fine frequency resolution, fast channel switching, and versatile modulation capability. These requirements are surpassing the performance capabilities of conventional analog phase-locked loops (PLLs). It is difficult for the conventional PLL-based frequency synthesizer to meet these requirements due to internal loop delay, low resolution, modulation problems, and the limited tuning range of the voltage-controlled oscillator (VCO). In contrast, a direct digital synthesizer (DDS) is capable of fast frequency hopping, fine frequency tuning, continuous-phase switching, direct modulation, arbitrary waveform, and quadrature signal generations. The advance of technology brings the device operating frequency to a higher level, increases the circuit density, and cuts down the manufacture cost. With the improvement of the technology, it becomes feasible to implement a single-chip DDS operating at millimeter-wave frequency at a reasonable cost, replacing the conventional analog PLL synthesizers in radar systems.

Though CMOS technology can be used to achieve better integration and reduce total cost, HBT technology is more favorable in microwave analog circuit design for its high current gain and low device noise in this frequency range. Two major candidates for high-speed DDS design are indium phosphide (InP) HBT and silicon germanium (SiGe) HBT technologies. The mobility of the carriers in InP devices is high and the cutoff frequency of the device can be well over 300 GHz, but the yield of complicated InP designs is still lower than those of other mature technologies. Taking the device performance, manufacture cost, and integration density into consideration, the SiGe process appears to be a better choice for DDS circuit design. Although there are several DDSs implemented in InP HBT technology that have been reported to work with clock frequencies from 9 to 30 GHz [1]–[3], the best power-efficiency figure-of-merit (FOM) of those DDSs is 2.4 GHz/W [2]. For comparison, the DDS presented in this study achieves a power-efficiency FOM of 5.04 GHz/W/phase. This DDS employs a 0.18-μm SiGe BiCMOS technology, which is less expensive, more compact, and consumes less power than its InP counterparts. The peak $f_s/f_{\text{max}}$ for the 0.18-μm SiGe HBT transistor is 120/100 GHz and the peak $f_s$ current for the minimum size transistor is less than 20% of that of the InP device [2]. The SiGe quadrature DDS described in this paper achieves a maximum clock frequency of 6.2 GHz with a power consumption of 2.5 W. Unlike aforementioned InP designs, which only provide single phase output, this DDS includes two sine-weighted current steering DACs to generate the accurate quadrature outputs simultaneously up to 3.1 GHz. To the authors’ best knowledge, this DDS is the only quadrature millimeter-wave DDS RF integrated circuit (RFIC) reported thus far.

This paper is organized as follows. In Section II, the direct modulations that can be implemented in DDSs are summarized. In Section III, the DDS circuit design is discussed. The layout issues that have a great impact on the final performance are addressed. In Section IV, the test platform and measured results are presented. Final conclusions are presented in Section V.

II. DIRECT MODULATIONS IN DDS

The conceptual diagram in Fig. 1 shows the method to implement different types of modulation configurations in a ROM-less DDS employing a nonlinear DAC. The principle of a DDS can be briefly described as first integrating the FCW into a phase control word, then mapping the phase control word to an amplitude word, and finally converting the amplitude word into...
an analog signal output. All the frequency, phase, and amplitude information are readily available in the DDS data path and can be directly addressed and manipulated, thus the digital modulation can be done without too much extra hardware cost. By directly using digital control words to change the values of registers in the data path of a DDS, the frequency, phase, and amplitude of the output waveforms can be precisely controlled. Since all the modulations are done in the digital domain, many disadvantages associated with normal analog modulations can be precluded. The values of the registers in a DDS are updated with a data rate that is equal to the input clock frequency, which means that high-speed modulated waveforms can be generated. Waveform generation for various modulation schemes is desired for novel radio transmitter architectures. As an example, modern radar systems place ever-increasing demand for affordable low-noise signals and high-speed waveform generation. With the availability of single-chip DDSs working at microwave frequency, digitally generating highly complex wide bandwidth waveforms at the highest possible frequency instead of down near the baseband would considerably reduce the transmitter architecture in terms of size, weight, and power requirements, as well as cost. These waveforms are used for high-range resolution radars in sorting targets from clutter with low probability of intercepting communication applications. The modulated waveform generation is a unique feature of the DDS approach. The DDS synthesizer can implement modulations and waveforms such as chirp, step frequency, FM, frequency shift-keying (FSK), minimum shift-keying (MSK), PM, AM, quadrature amplitude modulation (QAM), and other hybrid modulations, as illustrated in Fig. 1.

The typical choice converting the baseband signal from polar magnitude and phase data to Cartesian in-phase (I) and quadrature (Q) data during the modulation is based on the normal practical consideration. Direct manipulation of magnitude and phase in the polar system is expensive and difficult to design and build. The approach of taking a DDS into a transceiver system to perform the polar modulation task in addition to the normal frequency synthesis is one way to solve this problem that is worth further exploring. Since the major parts of a DDS are digital circuits, it is easier to integrate the DDS with a baseband circuit and it provides a compact solution to the transmitter design.

Sometimes it is expected that the DDS output can cover more frequency range, while the typical DDS output frequency ranges from dc to one-third of the input clock frequency. When the output frequency closes to the Nyquist output, the frequency of the alias image will come closer to the output frequency, which made it almost impossible to be removed with an analog low-pass filter. To build a low-pass filter with steep rolloff characteristic at several gigahertz will require tremendous effort. A practical solution to extend the output frequency of a DDS to a wider range without incurring the problems of alias images is to use a single sideband (SSB) mixer, as shown in Fig. 2.

The local oscillator generates quadrature outputs with relatively fixed output frequency $\omega_0$, which are mixed with the outputs of a quadrature DDS. The mixer outputs are then summed and subtracted with each other, thus the up-converted cosine waveforms with a frequency of $\omega_0 + \omega$ or $\omega_0 - \omega$ are derived. Theoretically, the final output should be clean of alias images. However, in practice, the DDS output contains harmonics and spurs that significantly deteriorate the purity of desired output waveforms. The imperfections of the mixers due to leakage and second-order effects will introduce some other spurs that have negative impacts on the output signals, even though the power of the alias image tune is small compared to the fundamental tune, which greatly eases the filter design. Assuming the local oscillator frequency is higher than the output frequency of the quadrature DDS, the above mixing scheme can be used to up-convert the DDS output frequency to a higher frequency band.

III. DDS CIRCUIT DESIGN

A. Quadrature DDS Architecture

The simplified block diagram of the ROM-less quadrature DDS, employing one 9-bit pipeline accumulator and two nonlinear DACs, is shown in Fig. 3. Intuitively, by paralleling two single-phase DDSs, one with sine output and another with cosine output, and then merging them together, a quadrature DDS can be realized. When performing the merger of two single-phase DDSs, the goal is to share the commonly used circuits in both DDSs as much as possible. In this design, the phase accumulator is shared for the two DDSs due to the limitation of fan-out factors of the digital logic gates at multigigahertz frequency, which leaves a very marginal gain when sharing the decoders and other digital blocks inside the DACs.

The main components in a single-phase ROM-less DDS are a phase accumulator and sine-weighted nonlinear DAC. For a DDS with an $I$-bit frequency control word (FCW) and $M$-bit...
phase resolution DAC, the output frequency of the synthesized sine waveform is $f_{\text{out}} = \left(\text{FCW}/2^L\right)f_{\text{clock}}$. The output of the phase accumulator is truncated into $M$ bits to fit the inputs of the nonlinear DAC. Usually, the phase resolution of the DAC is much less than the resolution of the phase accumulator, then $L-M$ bits are discarded, which introduces FCW dependent spurs. The contribution of phase truncation related spurs to the total spurs and the noise of the DDS output is considered to be a dominant factor if the following assumption is valid, that DAC is ideal, or close to ideal. However, even for a linear DAC, when the sampling rate is over multiple gigahertz and transition of the magnitude is larger compared to the full-scale output, the validity of the above assumption will no longer hold. For a nonlinear DAC, the situation is more complicated. It is not an easy task to reach high amplitude resolution with a nonlinear DAC at multiple gigahertz clock speed. In fact, the ultrahigh-speed nonlinear DACs in published studies, at most, have 8-bit amplitude resolution. The nonlinear DAC approach is still attractive for the microwave DDS design because it provides drastic speed improvement to the ROM- or algorithm-based DDS design. To reduce the effect of the amplitude error, introduced spurs in an ultrahigh-speed DDS need to be taken into account during the design. The phase truncation error introduced spurs are already minimized because only 1 bit of the phase accumulator output has been truncated.

As illustrated in Fig. 3, the quadrature DDS RFIC utilizes one 9-bit pipeline accumulator and two nonlinear 8-bit sine-weighted current-steering DACs to simultaneously generate the sine and cosine waveforms. The DDS comprises a 9-bit pipeline accumulator. Since the output frequency cannot exceed the Nyquist rate, an 8-bit FCW is fed into a 9-bit pipeline accumulator with the most significant bit (MSB) of the accumulator input tied to zero internally. Thus, the DDS requires only 8-bit FCW inputs. The output of pipeline accumulator gives a 9-bit phase word. The least significant bit (LSB) of the 9-bit phase word is truncated before driving the 8-bit DAC input.

To produce the 90° phase word a binary number of “01” needs to be added to the two MSBs of the DAC input. Translating the add function into the gate level, the output of the MSB is the result of an exclusive-OR (XOR) of the first two MSB inputs and the output of the second MSB is the inversion of the second MSB input. Since all the digital logics have differential outputs, only one XOR gate is needed to be inserted at the inputs of the sine-weighted DAC to convert it to a DAC with 90° output phase difference. A current steering DAC structure is chosen for its advantages of high speed and good matching between unit cells. The differential current outputs of the nonlinear current steering DAC are converted to differential voltage outputs with two pairs of external 15-Ω pull-up resistors. The detailed block diagram of the quadrature DDS is shown in Fig. 4. On the right side, there are two back-to-back sine-weighted current steering DACs, and on the left side, the phase accumulator is shared by both DACs. The DDS also includes a standard LC-tuned VCO, which can be connected to the input of the clock buffer on the upper side to drive the entire DDS. Since the two nonlinear DACs are identical, naturally it appears to be beneficial if all the decoders and buffers in the DACs can be shared, and only leave current switches and current sources separated. This is a plausible suggestion and worthy of further investigation. Before evaluating this alternative solution, the mechanism of the sine waveform generation in the nonlinear sine-weighted DAC will be explained.

The pipeline accumulator integrates the input FCW to phase information. Due to the symmetry of a sine waveform, only one-quarter of sine waveform data is stored in the sine-weighted DAC. The two MSBs are used to determine in which sine-wave quadrant the phase accumulator output resides according to the quadrant symmetry of the sine wave. The MSB output of the phase accumulator is used to provide the proper mirroring of the sine waveform at the $\pi$ phase point. The second MSB is used to invert the remaining 6-bit for the second and fourth quadrants of the sine wave prior to the decoding logic. The 6-bit outputs are split to 3 and 3 bits and fed into two column–row decoders, which drive column lines and row lines of the inputs of the current switch cells. Each column–row decoder in this circuit is a linear 3 : 8 operation. The outputs of the column–row decoder
go to the switch matrix to control the switches in each cell. The
latch and switch matrices contain 64 cells, and each is comprised
of a local decoder, latches, and switch pairs. The current weights
of the current sources inside the current source matrix are preset
to the sinusoidal waveform data. The current switch outputs are
summed at the open-collector output nodes.

Sharing all the digital blocks before current switch cells in
the DACs in order to reduce the circuit size or power consump-
tion may not have too much impact on the performance of the
DDS. The symmetry properties of the sine and cosine waveform
are different, particularly sine, which is an odd function and co-
sine, which is an even function. The turning on sequences of
the switch cells guarantee the complete sine-waveform gener-
ation. According to the symmetry property of the sine wave-
form, the derived cosine waveform is not continuous, as shown
in Fig. 5. Thus, directly sharing all the logic before the current
switch cells to simultaneous produce sine and cosine waveforms
will encounter some problems. One way to overcome the dif-
ficulty is to implement the XOR function, which generates the
first two MSBs input for the cosine DAC at the input into the
current switch cells. This method needs to add 64 or more logic
gates to the switching cells. Considering the fan-out factor of
the logic cells at several gigahertz, the total loads on the signal
paths are nearly the same. Thus, the actual number of gates are
not reduced, the area cost and power consumption will maintain
the same levels. It looks like sharing the logic blocks before the

B. Pipelined Accumulator

The adder in the phase accumulator of the DDS can be chosen
from various types such as pipeline, ripple-carry, and carry-
look-ahead adders. For modulation purposes, it would be ben-
eficial to use a carry-look-ahead adder or ripple-carry adder, but
their speeds are restricted by inevitably introducing more delay

Fig. 4. Detailed block diagram of the quadrature DDS.

Fig. 5. Output sine and cosine waveform depending on the symmetry property
of the sine waveform.

Sine

Cosine

0.5π 0 0.5π π 1.5π 2π

0.5π 0 0.5π π 1.5π 2π
stages in the critical paths. Instead, to achieve maximum operating speed, a pipelined accumulator is adopted in this design. The delays of the accumulators are determined by the propagation delay of the full adder (FA), the D-flip-flop (DFF), and the level shifter (LS), and can be expressed as

\[
T_{\text{total}}(\text{Pipeline}) = T_{\text{d}_p}(\text{DFF}) + T_{\text{d}_p}(\text{FA}) + T_{\text{d}_p}(\text{LS})
\]

\[
T_{\text{total}}(\text{Ripple-carry}) = T_{\text{d}_p}(\text{DFF}) + (T_{\text{d}_p}(\text{FA}) + T_{\text{d}_p}(\text{LS})) \times N.
\]

The total delay of the carry-looked-ahead accumulator has a delay between those two. From the above equations, it is clear that the pipeline accumulator can run at least double clock speed and is straightforward to build. The ripple adder topology uses the least hardware, but operates at the slowest speed. The delay of the carry-looked-ahead accumulator is estimated with a maximum fan-in of 3 and a group size of 3. For the DFF in the accumulator, a reset pin is added to reset the accumulator to the initial state.

In this DDS, a current mode logic (CML) cell has been chosen to implement the digital logic block. The breakdown voltage $V_{\text{CEO}}$ is 1.8 V and the $V_{\text{BE}}$ is approximately 0.9 V under a typical bias condition. For a three-level CML logic cell, to keep all the bipolar transistors working in the active region, the minimum power supply voltage is $V_{\text{SWING}} = V_{\text{BE}} + 2 \times V_{\text{CE,SAT}} + V_{\text{DS,SAT}}$, in which $V_{\text{SWING}}$ is the output amplitude of the CML. $V_{\text{CE,SAT}}$ is the saturation collector–emitter voltage of the SiGe bipolar transistor, and $V_{\text{DS,SAT}}$ is the saturation overdrive voltage of the nMOS transistor in the current source. Rough estimation indicates that the CML logic can work with a 2.7-V power supply, while speed will be sacrificed. 3.3 V is a more comfortable choice to ensure the base–collectors of all the bipolar junction transistors (BJTs) are reverse biased. The current source of the CML logic uses an nMOS transistor with a degeneration resistor to provide more headroom for the bipolar transistor operation. The overdrive voltage of an nMOS field-effect transistor (FET) is around 0.4 ~ 0.5 V, which is significantly smaller than a normal bipolar transistor. Choosing an optimized value of the bias current of the CML logic depends on several factors, i.e., the structure of this stage, total loads of the next stage, and the drive strength of the previous stage, which means the bias current for every logic gate should be separately tuned. A more practical approach is to choose the same bias current for the same type CML logic with equal size devices. Here the bias current is set to 70% of the peak $f_T$ current to achieve a good tradeoff between speed and power consumption. Although it will be more meaningful to use peak $f_{\text{MAX}}$ current to specify the operational speed, the peak $f_{\text{MAX}}$ is related to the load of the previous stage, a variable factor determined by the circuit itself. After all, the peak $f_T$ current can still serve as a reasonable indicator of average speed of the CML logic circuits. As a result, the propagation delay of the sum logic is 30 ps, and the carry block is 25 ps when setting a fan-out factor to 1 or 2.

C. DAC Current Source and Switch Circuits

The essential building block of the nonlinear DAC is the sine-weighted current-source matrix. The smallest unit current of each current source is 0.1 mA, which should provide the current switches with enough switching speed when toggling. The largest current in the current source is 0.7 mA, which is composed of seven identical current sources. The current switch contains two differential pairs, with minimal sized transistors, and a cascade transistor, to isolate the current sources from the switches and improve the bandwidth of the entire group of switching circuits.

The current source matrix provides 128 sine-weighted currents that are summed at the differential current outputs $\text{OUT}_P$ and $\text{OUT}_M$. The current outputs are converted to differential voltages by a pair of off-chip 25-Ω pull-up resistors. Fig. 6 shows that the currents from the cascode current sources are fed to outputs $\text{OUT}_P$ and $\text{OUT}_M$ by a pair of switches. The MSB controls the selection between parts A and B during different half periods. The size of the switching transistor pairs is chosen to be minimal in order to achieve the fastest switching speed, with minimum power consumption, and to reduce the effect of clock feed-through.

In the current steering DAC, the impedance $Z_{\text{imp}}$ seen in the drain of the switch transistors of each current cell must be large enough so its impact on the integral nonlinearity (INL) specification of the DAC can be tolerated [7]. However, $Z_{\text{imp}}$ is frequency dependent. To obtain 8-bit output resolution, $Z_{\text{imp}}$ should be approximately 500 kΩ. When the frequency increases above 100 MHz, a cascode current source is needed to meet the requirement for $Z_{\text{imp}}$.

Device matching is one of the important factors that affect the static and dynamic performance of the DAC. The matching properties of SiGe bipolar transistors are normally one order of magnitude better than those of MOSFETs with similar feature sizes. Carefully choosing current source transistor sizes.
and positions, and increasing the widths of the interconnections to reduce voltage (IR) drops helps to reduce matching errors. For those long interconnections carrying global signals like clock and MSB phase word, transmission line effects are taken into consideration during the layout. In order to minimize parasitic capacitances and inductances, top metal layers are used for global signal routings.

Power consumption of the DDS in the gigahertz range is always a severe problem due to the scale of the circuit and the high current density that the transistors require at these frequencies. To increase the operational speed, the current flow in the transistors should be increased proportionally to overcome both the transistor parasitic and interconnection loads. With a scaled-down device feature size, the latter plays a significant part in the total delay at relatively high speeds. The advantage of using bipolar transistors over their CMOS counterparts is that a bipolar transistor provides higher current gain while maintaining a reasonable size. The CMOS transistor area, on the other hand, is larger in order to generate the same amount current. The more meaningful specification of the bipolar transistor is \( I_{\text{max}} \), which takes into account the base resistance and provides insight into CML circuit speed under normal operation. The relatively high power density of DDS chips makes it extremely difficult to quickly remove heat without an external air flow. According to the ceramic package \( \theta_{JA} \) specification, it is quite normal to get a 20 °C \( \sim \) 30°C temperature increase per watt dissipation on the chip. If only the bare die area is considered, the situation is even worse because a total power of approximately 2 W would be concentrated on a small die area of 10 mm\(^2\). Thus, the indicated power density would exceed 100 W/in\(^2\), which is an alarming number and normally appears in only high-performance processors. Without a heat sink, the chip temperature could reach 85°C, with 27° of ambient temperature. For this reason, an external fan is used to cool down the device when making measurements.

D. Clock Tree and MSB Tree Designs

The most challenging parts of the design are the clock tree and MSB buffer tree designs. To eliminate glitches due to code errors induced by clock skews, clock trees are carefully balanced to ensure synchronization and drive capability. Since the differential clock signals drive every flip-flop cell, and the total number of flip-flops is above 200, synchronization of the clock signals is not a trivial task. With a clock input frequency around 10 GHz, the fanout ratio is only around 3 \( \sim \) 4, and thus, the depth of the clock buffer chain is at least 6. To fully turn on or turn off the differential bipolar pairs, the input differential peak-to-peak voltage swing should be more than \( 6V_T + I_E R_E \) in which \( V_T \) is the thermal voltage, 26 mV at room temperature, and \( I_E \) and \( R_E \) are emitter current and emitter resistance of the bipolar transistor, respectively. The voltage swing also depends on junction temperature, which can reach above 80 °C at the normal operation condition. The clock signals at the flip-flop cells should swing no less than 150 mV, which is equal to \( 6V_T \) at room temperature. Since every switching cell in the DAC has an MSB signal, the total number of gates to be driven exceeds 120. This MSB signal must also be synchronized with other decoded digital bits. The depth of the buffer chain for the MSB signal is 5. To accomplish all of this, the clock and MSB buffer require careful consideration in order to ensure that each middle and end point load are well balanced.

E. Layout Considerations

When running at a 10-GHz clock rate, layout plays an important role in assuring that the final design meets the expected speed requirement. The current source matrix and the switching matrix are separately laid out and isolated from one another using a deep oxide trench to reduce the noise coupling from the digital part to the current source from the substrate. The output of the DAC is placed close to the output pins to reduce the interference from the other parts of the circuit. Differential pair device signals are placed in a symmetrical manner such that the signal traveling lengths are almost same. In order to make the layout compact and easy to assemble, the CML building block has the same height, and power supply distribution stacks several metal layers to reduce the width of the metal.

Table I indicates the number of unit current sources in each sine-weighted current source. The sum of each row is the same,
which assures the regularity of the current source array, as well as its compactness. Cadence Skill language has been utilized to generate the connections, which form the unit current sources into the sine-weighted current sources, in accordance with the given switching sequence. Hence, the INL of the nonlinear DAC, due to symmetrical and gradient errors, is optimized.

In the layout, two dummy rows and columns have been added around the current source array to avoid edge effects. To minimize the systematic error, introduced by the voltage drop in the ground lines of the current–source transistors, sufficiently wide lines have been used. The clock inputs are differential CML compatible signals, and multiple clock inputs are provided to reduce the parametric inductance resulting from the pins. The maximum delay of the metal wire in chip is approximately 40 ps and the clock tree is carefully built to ensure an acceptable clock skew.
TABLE II
ULTRAHIGH-SPEED DDS PERFORMANCE COMPARISON. THIS WORK IS QUOTED FOR SINGLE-PHASE/QUADRATURE-PHASE DDS DESIGNS

<table>
<thead>
<tr>
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<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Emitter area of min size npn [µm²]</td>
<td>1.5x4</td>
<td>0.4x2</td>
<td>0.4x2</td>
<td>0.2x0.64</td>
<td>0.2x0.64</td>
</tr>
<tr>
<td>Peak fₚ current of min size npn [mA]</td>
<td>7.2</td>
<td>4</td>
<td>4</td>
<td>0.77</td>
<td>0.77</td>
</tr>
<tr>
<td>Quadrature phase outputs</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Accumulator size [Bit]</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>9</td>
<td>9</td>
</tr>
<tr>
<td>DAC resolution [Bit]</td>
<td>7</td>
<td>7</td>
<td>5</td>
<td>8</td>
<td>8</td>
</tr>
<tr>
<td>Max clock frequency [GHz]</td>
<td>9.2</td>
<td>13</td>
<td>32</td>
<td>12</td>
<td>6.8</td>
</tr>
<tr>
<td>SFDR [dBc]</td>
<td>30</td>
<td>26.67</td>
<td>21.56</td>
<td>30</td>
<td>26</td>
</tr>
<tr>
<td>Power consumption [W]</td>
<td>15</td>
<td>5.42</td>
<td>9.45</td>
<td>1.9</td>
<td>2.5</td>
</tr>
<tr>
<td>Transistors number</td>
<td>3000</td>
<td>1646</td>
<td>1891</td>
<td>9600</td>
<td>13500</td>
</tr>
<tr>
<td>Die size [mm²]</td>
<td>8x5</td>
<td>2.7x1.45</td>
<td>7.2x0.7</td>
<td>2.3x0.7</td>
<td>2.3x2.5</td>
</tr>
<tr>
<td>Power efficiency [Phase-GHz/W]</td>
<td>0.5</td>
<td>0.2</td>
<td>3.36</td>
<td>6.3</td>
<td>5.44</td>
</tr>
<tr>
<td>Area efficiency [DAC-Bit/mm²]</td>
<td>0.175</td>
<td>0.179</td>
<td>1.28</td>
<td>4.97 w. VCO</td>
<td>2.78 w. VCO</td>
</tr>
<tr>
<td>Tested prototypes</td>
<td>wafer</td>
<td>wafer</td>
<td>wafer</td>
<td>packaged</td>
<td>packaged</td>
</tr>
</tbody>
</table>

IV. MEASURED RESULTS

A die photograph of the quadrature DDS RFIC is shown in Fig. 7. This DDS design is quite compact with an active area of 2.3 × 2.5 mm² and a total die area of 3 × 3 mm². The DDS monolithic microwave integrated circuit (MMIC) was packaged in a 48-pin ceramic leadless package. The test board was built using a Rogers RO4003 laminate board, which has a loss tangent of less than 0.003 and good temperature stability. To convert the single-ended signal to differential clock inputs, a 180° 3-dB hybrid coupler is employed at the clock input. For the differential outputs, a second hybrid coupler is inserted into the output path to convert them into a single-end for testing. Fig. 8 illustrates the test setup.

We first tested the output of a single-phase DDS RFIC. In a separate design, we have implemented a single-phase DDS RFIC that was tested at a maximum clock frequency of 11 GHz with a power consumption of 1.9 W. At a Nyquist rate, the single-phase DDS can operate at a maximum clock frequency of 9.6 GHz, which corresponds to the record high power-efficiency FOM of 5.1 GHz/W [13]. Fig. 9 illustrates the measured single-phase DDS output spectrum with 2.227-GHz output and 9.07-GHz clock. The measured output power is approximately −16 dBm. All measurements were done without calibrating the losses of the cables and printed circuit board (PCB) tracks.

Figs. 10–13 illustrate the measured quadrature DDS output spectra and waveforms for different outputs and clock frequencies. Fig. 10 presents the 0.397-GHz quadrature DDS output spectrum with a 5.44-GHz clock input. The measured output power is approximately −4.67 dBm. Fig. 11 demonstrates the highest operational frequency of the quadrature DDS at 6.815 GHz with close to a Nyquist output of 3.394. The measured spurious-free dynamic range (SFDR) of the device, at a 3.394-GHz output frequency with a 6.815-GHz clock, is around 30 dBc. For Fig. 11, the FCW is chosen as 2^8 − 1, which is the maximum allowed by an 8-bit FCW input. Thus, the output frequency is set at \((2^8 - 1)/2^8 \times f_{\text{clk}} = 3.394\) GHz. The first-order image tone mixed by the clock frequency and the DDS output frequency occurs at 6.8 GHz − 3.387 GHz = 3.417 GHz, which is 27 MHz apart from the output frequency, as shown in Fig. 11. Operating the DDS at close to the Nyquist rate makes it very hard to filter out the image tones. Practically speaking, the DDS output frequency is restricted to be less than 3/8 of the clock frequency.

Fig. 12 illustrates the measured output waveform of the quadrature DDS outputs at 389 MHz with a 6.2-GHz clock. The time-domain waveform measurements were limited by the digital sampling scope’s 500-MHz bandwidth. Using a 6-GS/s sampling digital scope, Fig. 13 provides the output waveforms of the quadrature DDS RFIC with a 6.3-GHz clock input frequency and 1.58-GHz output. The measured I/Q waveforms demonstrate the 90° phase difference for the quadrature DDS RFIC outputs.

Table II provides a performance comparison of the recently published microwave-band DDS designs. The designs reported in [2] and [3] used InP technologies with an \(f_t/f_{\text{max}}\) above 300 above 300 GHz, which is almost triple those reported here. The InP DDS [1] employs an 8-bit accumulator and an 8-bit DAC and operates at a maximum clock frequency of 9.2 GHz with a power consumption of 15 W. On the other hand, the single-phase SiGe DDS [13] that has an 8-bit DAC and a 9-bit accumulator consumes only 1.9 W with 3.3- and 4-V power supplies for digital and analog circuits, respectively. For this design, the digital portion of the DAC consumes 300 mA and the accumulator consumes 250 mA under 3.3 V. The analog portion of the DAC consumes 35 mA using a 4.0-V supply voltage.

This paper presents the first millimeter-wave quadrature DDS design reported thus far [14]. The quadrature DDS RFIC contains more than 13 500 active devices with quite compact die
size. The active area of the quadrature DDS RFIC is approximately $2.3 \times 0.7 \text{mm}^2$, and its total die area is $3 \times 3 \text{ mm}^2$. When compared with other single-phase millimeter-wave DDSs [1],[2], this design achieves similar SFDR performance. It is more complex, yet more compact, and has lower power, as shown in Table II. The minimum size of the InP transistor is much larger than that of the SiGe transistor. Although the current density needed to achieve peak $f_{\text{r}}$ frequency in InP and SiGe technologies are similar, the current required to operate the minimum size SiGe transistor is much less. It is for this reason that the SiGe DDS leads to a superior power-efficiency performance.

V. CONCLUSION

This paper has presented a 9-bit 6.8-GHz low-power quadrature DDS implemented in 0.18-$\mu$m SiGe BiCMOS technology. The quadrature DDS RFIC occupies an active area of $2.3 \times 2.5 \text{ mm}^2$ and consumes a total of 2.5-W power. In a separate design, a 9-bit 9.6-GHz low-power single-phase DDS MMIC was implemented in 0.18-$\mu$m SiGe BiCMOS technology. The maximum clock frequency of the single-phase DDS MMIC was measured at 9.6 GHz with a power consumption of 1.9 W using 3.3-V/4.0-V dual power supplies. The DDS thus achieves a power-efficiency FOM of 5.1 GHz/W/phase. The DDS chips were measured in packaged prototypes using 48-pin ceramic leadless chip carrier (LCC) packages.

ACKNOWLEDGMENT

The authors would like to acknowledge D. Yang, Lattice Semiconductor Corporation, Bethlehem, PA, for layout of the accumulator and V. Kakani, Auburn University, Auburn, AL, for the VCO design. The authors would like to thank N. Albritton and B. Fieselman, both with the Amtec Corporation, Huntsville, AL, for business management, and J. Meinhardt, Kansas City Plant, Kansas City, MO, for fabrication support. The authors would like to thank E. Adler and G. Goldman, both with the Army Research Laboratory, Washington, DC, for supporting this project.

REFERENCES


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