A 5.2GHz Low Power Transceiver RFIC for WLAN Applications

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Abstract — This paper presents a low-power single chip WLAN 802.11a transceiver RFIC for personal communication terminal applications. The 5.2GHz transceiver RFIC is implemented in a 0.5µm SiGe technology with 16 mm² die size. It consumes 110/130mA in receive/transmit mode under a 3.3V supply. The receiver path shows a 6.4dB noise figure and a 20dBm IIP3 under a maximal 67dB gain. The transmitter path OIP3 is measured as 29.7dBm. The LC-tuned VCO has a tuning range from 4.08GHz to 4.7GHz and the measured phase noise is -112dBc/Hz @ 1MHz offset.

Index Terms — WLAN, 802.11a, SiGe, RFIC, low power, low noise, linearity, personal communication terminal.

I. INTRODUCTION

Wireless communications has attracted great attentions recently, fueled by the emerging of wireless local area networks (WLAN) and the third generation W-CDMA technology [1-6]. The ever-increasing demand for wireless multimedia applications such as video streaming keeps pushing future WLAN systems to support higher data rates (54 MBit/s up to 1 GBit/s) at high link reliability and over greater distances. Furthermore, the speed gap between "wired" and "wireless" LANs should be decreased so that WLAN can be seamlessly merged into high-data rate wired networks.

With WLAN standards operating in very different frequency bands, market leading WLAN solutions have to offer multi-mode interoperability with transparent worldwide usage. Moreover, the frequency allocation of the WLAN standards in the "unlicensed" 5-GHz band is constantly evolving. In particular, Japan proposed four additional RF channels in the 4.9 to 5.0-GHz band and further three channels in the 5.03 to 5.09-GHz band for this standard. This change could significantly increase the available channels for 5-GHz WLAN in Japan, and create yet another difficulty for WLAN chipmakers by requiring them to enable access to this lower-frequency band. It is thus desirable to design a WLAN transceiver with a future-proofed multi-band frequency synthesis scheme against evolutions and changes in allocated spectrum worldwide.

This paper represents a low-power and low-cost WLAN 802.11a transceiver RFIC for personal communication terminal applications. The 5.2GHz transceiver RFIC is implemented in a 0.5µm SiGe technology with 16 mm² die size. It consumes 110mA in receive mode and 130mA in transmit mode under a 3.3V supply. The receiver path provides a maximal 67dB and a minimal 20dB gain. The receiver path noise figure is measured as 6.4dB in maximal gain mode and its IIP3 is measured as -20dBm. The transmitter path OIP3 is measured as 29.7dBm. The LC-tuned VCO has a tuning range from 4.08GHz to 4.7GHz and the measured phase noise is -112dBc/Hz @ 1MHz offset.

II. TRANSCiever ArchiTEcTURE

Fig. 1 WLAN 802.11a transceiver RFIC block diagram.

Since the WLAN market is very cost-sensitive, for a competitive radio, it must be low cost and low power. Choosing the transceiver architecture wisely is thus critical. Superheterodyne radios require two synthesizers, but have a high level of transceiver performance. Their inherent frequency diversity reduces DC offset and VCO pulling effects as compared to direct conversion receivers. Although by comparison direct conversion receivers require only one local oscillator, often times mixing...
schemes are used to achieve similar frequency diversity, resulting in a more complicated transceiver. A compromise between the two approaches is to use a walking IF architecture where the RF LO is 4 times the IF LO [7]. Thus both LOs can be derived from a single synthesizer obtaining the benefit of a direct down conversion radio, but retaining the performance advantages of the superheterodyne radio.

The implemented transceiver RFIC is illustrated in Fig.1. The walking IF architecture is chosen because a single integer-N frequency synthesizer with a 16MHz reference would be enough to supply both RF and IF LO frequencies. In addition, only one VCO with wide-tuning range is needed to cover the 802.11a low and middle bands from 5.18GHz to 5.32GHz. The receiver includes a low noise amplifier (LNA) followed by an image filter to reject the RF image tone at about 3.2GHz. The RF mixer down-converts the received signal to IF frequency at about 1.05GHz. The IF mixers further demodulate the IF signal to baseband quadrature signals. The baseband block includes the VGAs for gain tuning and the baseband filter is off-chip. The transmitter starts with the baseband VGA blocks, followed by IF up-converters. The IF signal is further up-converted to 5.2 GHz signal by an RF mixer followed by an image filter. A pre-driver amplifies the 5.2GHz signal with -5dBm output power for driving the off-chip power amplifier.

II. RECEIVER FRONT-END DESIGN

Receiver front-end includes a differential LNA, an image-rejection filter and a down-converter mixer. The differential LNA has good noise performance and less dependence on the package parameters. Image-rejection filter is constructed with an inductor and two capacitors to remove the 3.2GHz image tones. RF mixer is also a differential structure to interface with differential LNA. Down-mixer output goes off-chip to a SAW filter, which has 1.05GHz center frequency and 30MHz bandwidth with 30dB out-of-band attenuations.

The circuit schematic of the mixer is shown in Fig. 2, which is a typical Gilbert cell with differential inputs and outputs. Inductor $L_{G}$ is used as emitter degeneration to increase the linearity of the mixer while consuming little voltage headroom. When $LO$ is ideal square wave, the mixer’s voltage gain is given by

$$A_v = \frac{2}{\pi} \frac{R_L}{r_e + j \omega L_C}$$

(1)

where $R_L$ is the load resistance and $r_e$ is the emitter resistance of $Q_2$ or $Q_5$. Since mixer’s IIP3 is proportional to $\omega C_{B} L_{G}$, $L_C$ should be carefully chosen to compromise between the gain and the IIP3. Noise matching is achieved by selecting the sizes of $L_5$ and the transistors and operating the RF transistors at the current density required for minimum noise figure. Combining with the matching network, $L_5$ also achieves simultaneous noise and power matching. Minimizing the noise of the mixer relies upon fast switching of the top quad-transistors. Note that the current in the quad switching transistors is identical to that flowing through the RF transistors below, where the bias current is tuned to the minimal noise figure current. Therefore, the top quad-transistors are sized such that their current density is close to that corresponding to the peak $I_{F}$. In this design, the ratio of the quad-transistor size to the RF transistor size is 1/6. The LO signals are applied to the base of the quad transistors through LO buffers, so that their amplitude can be kept large enough for completely switching. $L_4$ and $C_4$ are tuned to the LO+RF frequency to get rid of the unwanted sideband. The LC tank formed by $L_7$ and $C_7$ are tuned to the second RF harmonic, acts as a filtered current source in the emitter of the input transistors.

![Fig. 2 schematic of the up-mixer.](image)

III. TRANSMITTER DESIGN

A. Transmitter Baseband VGA

Transmitter variable gain stages attenuate the input signal by 0–30dB with a step size of 3 dB. Fig.3 illustrates the gain cell and the digitally controlled current sources. The receiver variable gain range is 36dB with a step size of 3dB. IQ modulator includes two mixers similar to the receiver IF mixers with image rejection. The summation of the quadrature mixer outputs is implemented by sharing the load resistors.
B. Power Amplifier Pre-Driver

The power amplifier driver consists of a differential cascade amplifier, an emitter follower, and a common-emitter amplifier as shown in Fig. 4. It is designed to drive the 50 Ω input of the off-chip 5.2GHz power amplifier. The degeneration inductors of the cascade amplifier help with the input matching of the PA driver, and they also trade the gain for linearity. The tanks are resonated at 5.2GHz, which provides 35dB image rejection for out-of-band tones.

IV. PLL FREQUENCY SYNTHESIZER DESIGN

In a walking-IF transceiver, the channel frequency is defined as $F_{ch} = RF + IF = 5180 + 20k$, where $k = 0,1,\ldots,7$ represents the 8 channels in WLAN 802.11a low and middle bands. The RF mixer has a local oscillation frequency (LO) at 4 times of the IF frequency, namely, $RF = 4IF = 4144 + 16k$. Thus, the VCO frequency is required to cover 4144MHz to 4256MHz for 802.11a low and middle bands. The IF frequency is given by $IF = RF/4 = 1036 + 4k$. Therefore, the walking IF is from 1036MHz to 1064MHz.

The integer-N phase lock loop (PLL) frequency synthesizer is shown in Fig. 5. It consists of an LC-tuned VCO which has a wide linear tuning range from 3.9GHz to 4.256GHz. Thus, the VCO can cover the entire 5.15–5.35GHz 802.11a bands. Schematics of the VCO is shown in Fig. 6, where P-MOSFETs are used for the oscillation transistors such that the tank can be referenced to the ground for low phase noise. The VCO design also employs an automatic-amplitude-control (AAC) circuitry that can keep the VCO in current-limit region and alleviate the AM and AM to PM noise. AAC also provides perfect ambient-proof characteristics over process, temperature and frequency variations.

In the PLL, an 8-bit programmable multi-modulus divider (MMD) is designed using the topology of cascaded 2/3 dual-modulus prescaler cell. The divide ratio can be programmed from 256 to 511. But only the 259 to 266 is used to generate the RF LO frequency from 4.144 to 4.256GHz. The IF LO frequency is a quarter of the RF LO frequency, which is achieved by twice dividing by 2.
operations. In this process, the I-Q LO signals for IF mixer can also be generated. The phase frequency detector (PFD) is a totally differential structure for symmetric and noise rejection. The charge pump (CP) is also differential and its current can be programmed from 200μA to 2.1mA for adjusting the loop gain. The control signal for MMD and programmable CP is input from a SPI data-loading interface.

IV. Measured Results

The 5.2GHz transceiver RFIC is implemented in a 0.5μm SiGe technology. Fig. 7 gives the die photograph of the transceiver RFIC, which occupies 16mm² areas and is packaged using a 48-pin leadless package. Fig. 8 gives the measured error-vector-magnitude (EVM) for typical IEEE 802.11a transmission with 64 QAM OFDM modulation. The measured EVM indicates that the presented transceiver meets the IEEE 802.11a OFDM requirement. Table I summarizes the WLAN transceiver performances. The receiver consumes 110mA current and the transmitter consumes 130mA current, respectively.

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<tr>
<th>TABLE I SUMMARY OF TRANSCEIVER PERFORMANCE</th>
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VI. Conclusion

This paper represents a low-power and low-cost SiGe RFIC WLAN 802.11a transceiver RFIC design for personal communication terminal applications. The transceiver meets the IEEE 802.11a OFDM requirement. The receiver consumes 110mA current and the transmitter consumes 130mA current under a 3.3V supply.

REFERENCES


