A 9-Bit 6.3GHz 2.5W Quadrature Direct Digital Synthesizer MMIC

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Abstract
This paper describes a 9-bit, 6.3GHz low power quadrature DDS implemented in a 0.18μm SiGe BiCMOS technology. With a 9-bit accumulator and two sine-weighted DACs, this DDS is capable of generating quadrature sinusoidal waveforms up to 3.15GHz. The quadrature DDS MMIC occupies an active area of 2.3x2.5mm² and consumes a total 2.5W power.

Keywords: DDS, SiGe, waveform generation, frequency synthesis.

Introduction
The advances in communication and radar systems are placing increasing demands on low power waveform generation and versatile modulation capability for frequency synthesis. A direct digital synthesizer (DDS) microwave monolithic IC (MMIC) is capable of fast frequency hopping, fine frequency tuning, continuous-phase switching, direct modulation, arbitrary waveform and quadrature signal generation. Recently, DDS designs have been reported with clock frequencies from a few GHz to 32GHz [1][2][3]. All the mm-wave DDS MMICs reported so far are single phase DDSs. Most of the mm-wave DDSs have been implemented in InP technology, and the best power efficiency figure-of-merit (FOM) reported so far is 2.4GHz/W [2].

The DDS described herein employs 0.18μm SiGe BiCMOS technology, which is less expensive, more compact and consumes much less power than its InP counterparts. As a result, the SiGe DDS design in this paper achieves a maximum clock frequency of 6.2GHz with a power consumption of 2.5W and includes two sine-weighted digital-to-analog converters (DAC) to generate the quadrature outputs. The power efficiency FOM is 5.04GHz/W/Phase. To authors' knowledge, this DDS MMIC is the only quadrature mm-wave DDS MMIC reported so far. In a separate design, we have implemented a single-phase DDS MMIC that was tested at a maximum clock frequency of 11GHz with a power consumption of 1.9W. At Nyquist rate, the single phase DDS can operate at a maximum clock frequency of 9.6GHz, which corresponds to the record high power efficiency FOM of 5.1GHz/W.

Ultra-High Speed DDS Designs
In this design, the ROMless structure with two nonlinear current steering DACs is employed, and the sine/cosine mapping function is performed by a sine-weighted DAC instead of using the traditional ROM-based sine waveform look-up-table. By eliminating the ROM, speed of the DDS is improved and the power consumption is reduced. This quadrature DDS comprises a 9-bit pipeline accumulator and two 8-bit sine-weighted current-steering DACs, as shown in Fig. 1. To produce the 90 degree phase, an XOR gate is inserted into the inputs of one sine-weighted DAC. Since the output frequency cannot exceed the Nyquist rate, an 8-bit frequency control word (FCW) is fed into a 9-bit pipeline accumulator with the MSB of the accumulator input tied to zero. The LSB of the 9-bit phase word is truncated, and its MSB is used to provide the proper mirroring of the sine waveform about the π phase point. Its 2nd and 4th quadrants of the sine wave prior to the decoding logic. The outputs of 3:8 column-row decoders go to the switch matrix to control the switches in each DAC cell. The latch and switch matrices contain 64 cells.

In order to achieve a good balance between speed and power consumption, the CML tail bias current is set to 70% of the peak fT current. The peak fT current for the minimum size SiGe transistor is less than 1/5 of that of the InP device [2]. This bias current is sufficient to keep the delay of the three-level gates below 25ps. To reduce the clock skew, clock trees are carefully balanced to ensure synchronization and drive capability. Since every switching cell in the DAC has an MSB signal, the total number of gates to be driven exceeds 240. This MSB signal must also be synchronized with other decoded digital bits. The unit current of each DAC current source is 0.1mA, while the largest current in the current source is 0.7mA. The current outputs are converted to differential voltages by a pair of off-chip 20Ω pull-up resistors. Fig. 2 shows that the currents from the cascade current sources are fed to outputs OUTp and OUTn by pairs of switches. The DDS also includes an LC-tuned VCO, which can be used as an internal clock.
Measured Results

The die photo of the DDS MMIC is shown in Fig. 3. This DDS design is quite compact with an active area of 2.3x2.5 mm² and a total die area of 3 x 3 mm². The DDS MMIC was packaged in a 48-pin ceramic leadless package. The test board is built using Rogers RO4003 laminate, which has a loss tangent of less than 0.003 and good temperature stability. To convert the single-ended signal to differential clock inputs, a 180 degree 3dB hybrid coupler is employed at the clock input.

Fig. 4 illustrates the measured single-phase DDS output spectrum with 2.227GHz output and 9.07GHz clock. The measured output power is approximately -16dBm. All measurements were done without calibrating the losses of the cables and PCB tracks. Fig. 5 illustrates the output waveforms of the quadrature DDS MMIC with a 6.3GHz clock input frequency and 1.58GHz output. Using a 6GS/s sampling digital scope, the measured I/Q waveforms demonstrate the 90 degree phase difference.

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References

