RFIC Design for Wireless Communications

VLSI Design & Test Seminar, April 19, 2006

Foster Dai

1. An MIMO Multimode WLAN RFIC

2. A $\Delta\Sigma$ Direct Digital Synthesizer IC
An MIMO Multimode WLAN RFIC

1. An Overview of MIMO Technology

2. MIMO Transceiver Design

3. Transceiver Building Block Circuits

4. Measured Results

Advantages of MIMO Technology

- MIMO can extend range and higher data rates
- Graph shows that for a 4X4 MIMO system 16.5dB less S/N ratio required for 54MBit/sec compared to standard technology
- As well vector CBF is shown which uses four orthogonal data streams to increase data rate 4X.
- VCBF not implemented here (not backwards compatible), but shows future of this technology.
MIMO Transceiver Design

Two Radios On the same chip

Beam Forming in the TX to get antenna gain through signal shaping

Master Chip

Slave Chip

LO Porting Trace

Link

Maximum ratio Combining at receive of signals in four paths at the RX

Master Chip

Slave Chip

LO Porting Trace

Note: Both beam forming and maximum ratio combining controlled by DSP

Transmitting Radio

Receiving Radio

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MIMO Transceiver Design Issues

MIMO transceiver RFIC design is a challenge due to the following issues:

1. Multiple radios on same die cause interference, especially PAs cause VCO injection-locking. Careful floor planning and proper isolation in layout are critical. VCOs operate at different frequencies from the PAs.

2. All LOs must be synchronized. MIMO calibration requires loop back measurement to match phase and amplitude of all paths.

3. Tx-Tx isolation must be high to maximize the gain from CBF. 30dB or higher desired.

4. Rx-Rx isolation must be maximized in order to maximize the gain from MCR. 40dB desired.
• Uses walking IF architecture for only one synthesizer
• Includes 2 a/b/g paths on each chip.
• Either master or slave PLL mode.
• BB filters switched so same Si used in Tx and Rx.
Synthesizer Design

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Chip Layout

- Designed in a 50GHz SiGe BiCMOS technology
- Chip measures 5.4mmX5.4mm
- Placed in a 72pin leadless plastic chip carrier (LPCC) package.
EVM Measurements

Shows typical EVM measurement which complies with IEEE 802.11a standard.

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Synthesizer Phase Noise Measurements

- Shows good agreement with measured results.

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### Summary of Transceiver Performance

<table>
<thead>
<tr>
<th>Parameter</th>
<th>802.11b/g</th>
<th>802.11a</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Band</strong></td>
<td>802.11b/g</td>
<td>802.11a</td>
</tr>
<tr>
<td><strong>Technology</strong></td>
<td>0.5µm SiGe BiCMOS</td>
<td></td>
</tr>
<tr>
<td><strong>Voltage Supply</strong></td>
<td>2.75V</td>
<td>2.75V</td>
</tr>
<tr>
<td><strong>TX Chain Current Supply (1path/2paths)</strong></td>
<td>240/400mA</td>
<td>255/430mA</td>
</tr>
<tr>
<td><strong>RX Chain Current Supply (1path/2paths)</strong></td>
<td>195/320mA</td>
<td>195/320mA</td>
</tr>
<tr>
<td><strong>Synthesizer Current supply</strong></td>
<td>36mA</td>
<td>36mA</td>
</tr>
<tr>
<td><strong>TX output power</strong></td>
<td>11dBm</td>
<td>13.5dBm</td>
</tr>
<tr>
<td><strong>EVM at TX output power</strong></td>
<td>4% (g only)</td>
<td>4%</td>
</tr>
<tr>
<td><strong>TX Path to Path Isolation (measured at the PA outputs)</strong></td>
<td>&gt;40dB</td>
<td>&gt;40dB</td>
</tr>
<tr>
<td><strong>RX NF @ Max Gain</strong></td>
<td>4.1dB</td>
<td>7.5dB</td>
</tr>
<tr>
<td><strong>RX chain Max Gain</strong></td>
<td>77dB</td>
<td>72dB</td>
</tr>
<tr>
<td><strong>RX chain Min Gain</strong></td>
<td>5.5dB</td>
<td>25dB</td>
</tr>
<tr>
<td><strong>Rx IIP3 @ Min Gain</strong></td>
<td>+8.8 dBm</td>
<td>-12.8 dBm</td>
</tr>
<tr>
<td><strong>RX I/Q Amplitude Imbalance</strong></td>
<td>0.3 dB</td>
<td>0.3 dB</td>
</tr>
<tr>
<td><strong>RX I/Q Quadrature Error</strong></td>
<td>2.0°</td>
<td>2.0°</td>
</tr>
<tr>
<td><strong>RX Path to Path Isolation (measured at the BB filter output)</strong></td>
<td>&gt;50dB</td>
<td>&gt;40dB</td>
</tr>
<tr>
<td><strong>Max DC offset without correction (measured at the output of the BB filter)</strong></td>
<td>90mV</td>
<td>90mV</td>
</tr>
<tr>
<td><strong>Synthesizer Integrated Noise 100Hz to 10MHz</strong></td>
<td>0.35~0.43° rms</td>
<td>0.63~0.86° rms</td>
</tr>
<tr>
<td><strong>VCO Phase Noise</strong></td>
<td>-120dBc/Hz @ 1MHz</td>
<td>-120dBc/Hz @ 1MHz</td>
</tr>
<tr>
<td><strong>In Band Phase Noise</strong></td>
<td>-98dBc/Hz @ 10kHz</td>
<td>-98dBc/Hz @ 10kHz</td>
</tr>
<tr>
<td><strong>Synthesizer Reference Frequency</strong></td>
<td>40MHz</td>
<td></td>
</tr>
<tr>
<td><strong>Synthesizer Step Size</strong></td>
<td>468.75kHz</td>
<td>781.25kHz</td>
</tr>
<tr>
<td><strong>Synthesizer Spurious</strong></td>
<td>&lt;-50 dBc</td>
<td></td>
</tr>
</tbody>
</table>
A Multi-Band $\Sigma\Delta$ Fractional-N Frequency Synthesizer

Demo of Range Improvement Using the MIMO Transceiver RFIC

Shows improved range of MIMO radios in an office building at 2.4GHz. 4X4 link range too large to show.

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Conclusions

• Implemented an IEEE 802.11a/b/g transceiver RFIC for 2.4GHz and 5.2GHz and Japan 4.9GHz multi-band MIMO WLAN applications.

• Transceiver RFIC includes two complete radio paths fully integrated on the same chip.

• Using walking IF architecture, uses a single $\Sigma\Delta$ fractional-N synthesizer for LO generation.

• Using two RFICs, 4X4 MIMO radio link has been tested under a typical indoor WLAN environment.

• The measured 4X4 MIMO radio achieves 15dB of link margin improvement over a conventional SISO radio.
A CMOS Direct Digital Frequency Synthesizer with Single-Stage SD Interpolator and Current-Steering DAC

- DDS spurs and quantization noise due to phase truncation.
- Frequency domain and phase domain $\Sigma\Delta$ noise shaping schemes.
- 12-bit current-steering DAC with $Q^2$ random walk switching scheme.

Conventional ROM-Based DDS

Fine step size requires a large accumulator and a large ROM. To reduce ROM size, the phase word is truncated, causing spurs at DDS output.

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DDS Pros and Cons

• Advantages
  Fine frequency tuning resolution
  Fast frequency switching
  Quadrature outputs with accurate I/Q matching
  Direct modulations (PSK, FSK, MSK, PM, and FM)
  Compatible with digital CMOS processing

• Disadvantages
  Low output frequency
  Quantization noise and spurious tones
Using a 4th order $\Sigma\Delta$ modulator, ROM sized is reduced by a factor of 16 times, without compressing the ROM.

ROM size can be further reduced using ROM compression algorithms.

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Output Spectrum Before Deglitch Filter

For DDS With 4th Order $\Delta\Sigma$ Modulator

(a) Simulated

(b) Measured

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Comparison of Measured Output Spectra for DDS with and without The 4th Order ∆Σ Modulator

With ∆Σ

SFDR improved by 14 dB

Without ∆Σ

72 dB

58 dB

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Die Photo of The ∆Σ DDS Prototype

Implemented in 0.35μm CMOS Technology

Die area = 2.2 × 2mm²

DDS core = 1.11mm²
ΣΔ accumulator = 0.3 × 0.2mm²
ROM = 0.3 × 0.3mm²
  ROM size is greatly reduced
due to the use of ΣΔ.
DAC = 0.6 × 1.6mm²

Power consumption = 200mW
DAC = 82 mW
Vdd = 3.3V
Max clock frequency = 300MHz
Questions?

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