Overview of Virtex 4 & Virtex 4 BIST Project
FPGA Testing Challenges

- Programmability
  - Must test all modes of operation

- Architectures designed for applications
  - Testability is after thought
  - Left to product/test engineers

- Constantly growing size
  - Reconfiguration dominates test time

- Constantly changing architectures

- Incorporation of new and different cores
Xilinx Virtex 4 FPGAs

- Array of 1,536 to 22,272 PLBs
  - 4 LUTs/RAMs (4-input)
  - 4 LUTs (4-input)
  - 8 FF/latches

- 48 to 552 18K-bit dual-port RAMs
  - Also operate as FIFOs
  - Also operate as 36K-bit RAMs with ECC (Hamming)

- 32 to 512 DSP cores 48-bits

- 0 to 2 PowerPC processor cores
Virtex 4 BIST Project

- BIST for CLBs = Sachin Dhingra
- BIST for I/O Buffers = Sudheer Vemula
- BIST for RAMs & DSPs = Daniel Milton
- Guard Band (w/BIST) = Lee Lerner
- BIST for Interconnect = Chuck Stroud
- Project scheduled for completion this year
Logic BIST for Virtex 4 FPGAs Using Embedded Microprocessor

VLSI Design & Test Seminar - January 2006
Outline

- Introduction
- Partial Configuration Readback
- Comparison
  - Virtex 2 Pro
  - Virtex 4
- Logic BIST Using Embedded Processor
  - PowerPC/Microblaze
  - New approach
- Circular Comparison BIST Architecture
Introduction

- **Built-In Self Test (BIST) for FPGAs**
  - Program some Programmable Logic Blocks (PLBs) as Test Pattern Generators (TPGs) and Output Response Analyzers (ORAs) to test the remaining resources of the FPGA
  - Diagnosis and Fault Tolerant Operation
  - No area overhead

- **Issues**
  - Large number of Configurations => High memory requirements
  - Slow Configuration Speeds => Long test times

- **Proposed Solutions**
  - Partial Reconfiguration
  - Partial Configuration Memory Readback
  - BIST using Embedded Processor
Partial Configuration Memory Readback

- Recent FPGAs allow configuration memory readback of only a section of FPGA
- Column based configuration memory using frames spanning entire columns
- Only the frames containing BIST results are read
  - Frames for FFs in ORA columns only
  - Time saved compared to Full Configuration Memory Readback
- Saves Logic & Routing resources
  - Scan Chain is absent

Diagram:
- Empty PLB
- Block Under Test (BUT)
- Output Response Analyzer (ORA)
- Test Pattern Generator (TPG)
- ORA Flip-Flop
Comparison of V2P and V4 for Logic BIST

<table>
<thead>
<tr>
<th></th>
<th>Virtex 2 Pro</th>
<th>Virtex 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>PLB</td>
<td>All four Identical slices</td>
<td>2 slices of 2 types</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SliceL (logic) &amp; SliceM (memory)</td>
</tr>
<tr>
<td>XDL</td>
<td>Row-Column CLB co-ordinates</td>
<td>XY CLB co-ordinates</td>
</tr>
<tr>
<td></td>
<td>Minor changes from Virtex I</td>
<td>Similar to V2P w/ minor changes</td>
</tr>
<tr>
<td>Location of 2 PPCs</td>
<td>Left and Right Halves</td>
<td>Top and Bottom Halves</td>
</tr>
<tr>
<td>Slice Testability</td>
<td>Poor</td>
<td>Better</td>
</tr>
</tbody>
</table>
BIST Using Embedded Processor

- Embedded Processor runs BIST and diagnosis
  - PowerPC
  - Microblaze

- No dedicated resources for embedded processor
  - FPGA resources are required for interface to
    - Program memory (block RAMs)
    - Internal Configuration Access Port (ICAP)
    - UART (hyper-terminal interface to PC)

- Read-Modify-Write using ICAP module
  - Fast partial reconfiguration
  - Verification and debug procedure for development
  - Fault injection emulation

- FPGA is divided in two sections for testing:
  - Embedded Processor
  - BIST circuitry
Embedded Processors in V2P

- Microblaze - Soft Core
  (Can be placed anywhere on the device)

- PowerPC - Hard Core
  (Fixed position in a device)
## Comparing Embedded Processors

<table>
<thead>
<tr>
<th></th>
<th>Microblaze</th>
<th>PowerPC</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Location</strong></td>
<td>Variable – can be located anywhere in FPGA</td>
<td>Fixed - hard core has fixed location in FPGA</td>
</tr>
<tr>
<td><strong>Availability</strong></td>
<td>all Virtex 2, Virtex 2 Pro, Virtex 4 devices</td>
<td>Selected Virtex 2 Pro and Virtex 4 FX only</td>
</tr>
<tr>
<td><strong>Speed</strong></td>
<td>200 MHz (max)</td>
<td>450 MHz (max)</td>
</tr>
<tr>
<td><strong>Compiler</strong></td>
<td>EDK</td>
<td>EDK</td>
</tr>
<tr>
<td><strong>Slice count</strong></td>
<td>1000</td>
<td>1035</td>
</tr>
<tr>
<td><strong>Slice count</strong></td>
<td>900</td>
<td>820</td>
</tr>
<tr>
<td><strong>BRAM count</strong></td>
<td>40</td>
<td>36</td>
</tr>
<tr>
<td><strong>BRAM count</strong></td>
<td>16</td>
<td>16</td>
</tr>
</tbody>
</table>

* Processor type is EDK compiler option - same code works for both Microblaze and PowerPC without any modifications

** Compacted Design
BIST Architecture

- BIST in part of the FPGA
- Embedded Processor occupies rest
  - Hard core or
  - Soft core (easier to move)
- Embedded processor also consists of peripheral devices:
  - UART
  - Memory interface
  - BUS arbiter
  - ICAP Module
- BIST and processor swap places for next test session
Logic BIST Architecture

- **Four Test Sessions**
  - Right Half – East
  - Right Half – West
  - Left Half – East
  - Left Half – West

- **Two Test Slice sets for V2P**
  - Only 2 of 4 slices can be tested in one configuration

- **Single Test Slice set for V4**
  - More testable slice architecture

- **Diagnostic Resolution**
  - Depends on ORA design and connections to BUTs

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1/18/06 VLSI Design & Test Seminar

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Circular Comparison Logic BIST

- **Architecture**
  - TPG moved to processor portion of FPGA
  - Can be performed by processor
  - ORA column instead of TPGs
  - Circular comparison of BUTs

- **Higher diagnostic resolution**
  - BUTs on the edges are now compared by two ORAs

- **Needs sufficient routing resources**
Virtex 2 Pro (XC2VP30)
Circular Comparison Logic BIST

- Microblaze
- Block RAMs
- Circular Comparison BIST Circuitry
- TPGs (inside the processor half)
Defining Area Constraints

Area constraints defined using XDL

BIST Circuitry

Microblaze

Block RAMs

Area Constraints defined using PACE
Virtex 4 FX12 with Logic BIST
Logic BIST for V4 SliceL

Fault Coverage (FC)

# Faults Detected

Configuration #

# Faults Detected

Configuration #

Individual FC

Cumulative FC

FC (%)

Individual FC

Cumulative FC
Summary & Conclusions

- Processor of choice: Microblaze
  - Reconfiguration
  - Results retrieval
  - Diagnostics

- Better testability of PLBs in V4 architecture
  - Higher diagnostic resolution
  - Fewer Configurations

- Circular Comparison Logic BIST possible due to abundance of routing resources

- Lesser details about the architecture
  - Increased development time
Built-In Self-Test for Programmable I/O Buffers in FPGAs and SoCs

Sudheer Vemula
FPGAs consist of
- Programmable Logic Blocks (PLBs)
- Routing Resources
- Interconnect points
- I/O Buffers

BIST configurations have been developed to test logic and routing resources in the core of an FPGA.

BIST configurations were not developed to test the I/O (Input/Output) buffers in an FPGA.
Types of I/O Buffers

- Every I/O Buffer can be:
  - Input
  - Output
  - Bi-directional

- Connections
  - Bonded I/O
  - Unbonded I/O

- Types (in some FPGAs)
  - Primary I/O Buffer
  - Secondary I/O Buffer
  - Clock Buffer

- Connections (in some FPGAs)
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Architecture of Atmel I/O Buffer
Resources in I/O Buffer

- I/O buffers have several programmable features
  - Multiplexers
  - Flip-flops or Latches
  - Pull-up, Pull-down capabilities
  - Delays, Slew rate, I/O Standards
  - Drive capabilities, Tri-state enable
  - Transmission Gates
  - Global Reset Connection
Basic Testing Approach

from TPG to ORA

from TPG to ORA

1/18/06
General I/O Buffer BIST Architecture

- TPG may be a counter or an LFSR
- ORA is comparison-based to latch mismatches due to faults
- Output of each I/O buffer is compared by two ORAs with the outputs of two other buffers
- Circular comparison improves diagnostic resolution
Manufacturing vs. In-System Test

- In Manufacturing test all the bonded and unbonded IOBs can be tested
  - Independent of package
  - Routing associated with the IOBs can also be tested

- In system level testing only the output buffers are tested
  - Testing the input buffers will back drive them
Atmel Implementation

- 3 BIST configurations developed using MGL
  - Configurations test
    - primary I/O
    - secondary I/O
    - global reset in primary and secondary I/O
  - Subsequent BIST configurations via dynamic partial reconfiguration from AVR
    - 12 for primary I/O
    - 9 for secondary I/O
    - Approximately 2x3N for global reset
      - N = # PLBs in one dimension of NxN array
      - N=24 for AT94K10
      - N=48 for AT94K40

- AVR dynamic partial reconfiguration reduces test time
  - Particularly when testing global reset
Fault Simulation Results for AT94K

100% fault coverage is obtained with additional configuration for global reset.

BIST Configurations

Fault Coverage (FC)
Atmel Summary

- Number of BIST configurations for I/O buffers is high
  - Compared to 16 for logic BIST and 48 for routing BIST
- Can achieve 100% gate level stuck-at fault coverage
- Major defects in analog circuitry of IOB are detected in both the approaches
  - Parametric faults like $V_{OL}$, $V_{OH}$, delay defects, current sink and source capabilities may not be detected
I/O Buffers in Virtex 4

- Every I/O Buffer consists of:
  - ILOGIC (Input Logic)
  - OLOGIC (Output Logic)
  - PAD

- IOBs are paired to be able to operate as a differential pair.
  - Each can be accessed individually in Single Data Rate (SDR) mode.
ILOGIC Block

- Gets input from the pad
- Consists of
  - 64 tap delay element (variable or fixed)
  - Flip-Flops (registered outputs and Double Data Rate (DDR) registers)
  - 3 different outputs
    - Unregistered direct connection
    - Different modes of operation of DDR registers
- Only upper register can be configured as either Flip-Flop or latch
IDDR Modes and ISERDES

- IDDR registers can be operated in 3 modes
  - Opposite Edge Mode (2 registers)
  - Same Edge Mode (3 registers)
  - Same Edge Pipelined mode (4 registers)

- ILOGIC block can also be operated in input serial-to-parallel mode

- ISERDES can be operated in either Single Data Rate (SDR) or DDR mode
  - SDR Mode – Creates 2-8 bit parallel word
  - DDR Mode – Creates 4, 6, 8, or 10-bit parallel word
OLOGIC Block

- Sources output to the pad
- 6 storage elements
  - 3 for tri-state control
  - 3 for output data
  - Both sets of registers have same functionality
  - Only upper register can be configured as either Flip-Flop or latch

OLOGIC Block in the FPGA Editor
ODDR Modes and OSERDES

- ODDR registers operate in 3 modes
  - Opposite Edge Mode (2 registers)
  - Same Edge Mode (3 registers)
- OLOGIC block can be operated in output parallel to serial converter mode
- OSERDES can be operated in either Single Data Rate (SDR) or DDR mode
  - SDR Mode – Converts 2-8 bit parallel word to serial
  - DDR Mode – Converts 4, 6, 8 or 10-bit parallel word to serial
Summary

- A BIST approach to test the programmable IOBs of any FPGA or FPGA core in an SoC
- Implementation results for the Atmel IOBs
- Architecture of the IOBs in Xilinx Virtex-4 FPGAs
  - BIST configurations are being developed for Virtex-4
- Publications
  - Vemula & Stroud, “BIST of I/O Buffers in Atmel FPGAs”, IEEE North Atlantic Test Workshop, 2005
  - Vemula & Stroud, “BIST for Programmable I/O Buffers in FPGAs and SoCs”, IEEE Southeastern Symp. on System Theory, 2006