Graduate Course for Spring 2002
TESTING OF
ULTRA LARGE SCALE INTEGRATED CIRCUITS
16:332:576
Section 01 Index Number 66047

Prof. Michael L. Bushnell – Rutgers University
Prof. Vishwani D. Agrawal – Agere Systems Lab. and Rutgers University
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This course covers the problems of testing of Ultra Large Scale Integrated Circuits (ULSI), the
design of circuits for testability, the design of built-in self-testing circuits, and the use of the IEEE
Boundary Scan Standards. IBM’s ULSI circuits contained 50 million transistors in 2000. Testing
determines whether a manufactured ULSI circuit contains any broken wires or transistors. Design
for Testability is necessary, since testing has become so difficult that we must explicitly synthesize
circuits to be testable and testing must be considered during all design phases. Testing of circuits
is currently one of the most critical obstacles to designing microprocessors and Application Specific
Integrated Circuits (ASIC’s). Chip designers, who want to learn about design for testability in order
to design better chips, and researchers, who wish to develop algorithms and patents for testing,
should take this course. Currently, verification testing and production testing represent 50 to 60 %
of the cost of making VLSI chips, and are now the biggest cost of this technology. The course will
be presented as a series of lectures, and each student will have to give a half hour in-depth lecture
on a topic that he/she has researched in the literature. In addition, each student will have to turn
in a well-researched and well-written paper on his topic. The level of this course is appropriate for
a college senior or a first year graduate student with experience in Digital Electronics Design. The
course will meet once a week, for three hours. Agrawal and Bushnell have finished a new testing
book based on this course, which will be used this year.

PROFESSORS: Michael L. Bushnell Room 624, CORE Bldg.
Vishwani D. Agrawal Room 611, CORE Bldg.

Bushnell’s Telephone: (732)445-4854
Bushnell’s Email Address: bushnell@caip.rutgers.edu
FAX: (732)445-4775
Agrawal’s Telephone: (908)582-4349
Agrawal’s Email Addresses: va@agere.com
Bushnell’s Office Hours: Tuesday 2:00-6:00
Meeting Room: Room 216, SEC Building
Meeting Time: Friday, 9:20-12:30 a.m.
First Meeting: Friday, Jan. 25, 2002
Course Completion Date: May 15, 2002
TEXT:


REFERENCE BOOKS:

- See Appendix C of the Bushnell & Agrawal textbook.

ASSUMED BACKGROUND:

<table>
<thead>
<tr>
<th>Boolean Algebra</th>
<th>Combinational Circuit Logic Design</th>
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<tr>
<td>Sequential Circuit Logic Design</td>
<td>College Sophomore Electrical Network Theory</td>
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<td>C and C++ Language Programming</td>
<td>RISC Computer Architecture</td>
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WORK EXPECTED OF STUDENTS. The course will meet once a week, for three hours, for 13 weeks. There are a series of lectures that each student is expected to attend. Each student will have to complete all of these items:

1. A twenty minute in-depth presentation on a testing topic that he/she has researched in the literature. The student talk must SUPPLEMENT, not REITERATE, material presented by the main lecturer(s). Please prepare viewgraph transparencies so that your talk goes faster.

2. An individual programming or design project, in which he/she writes part of a Computer-Aided Design program for circuit testing in C++, or develops a testing circuit. The programming project must be demonstrated to the rest of the class at the term end.

3. Thirteen homework assignments on the various test-pattern generation algorithms and on the structure of scan-design and built-in self-testing circuits.

4. A well-researched and well-written paper (of at most 6 pages) describing his/her topic, with proper literature citations. Badly written papers will be returned to you for rewriting. For examples on how to correctly write technical papers, look at the papers cited in Bushnell and Agrawal.

5. A final examination.
TENTATIVE SCHEDULE OF TOPICS:

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<tr>
<th>Topic</th>
<th>Reading Chapter</th>
<th>Lecturer</th>
<th>Date</th>
<th>Homework</th>
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<tr>
<td>Test Introduction &amp; Test Equipment</td>
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<td>Agrawal</td>
<td>2/8/02</td>
<td>3</td>
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<tr>
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<td>Combinational ATPG (Continued)</td>
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<td>Bushnell</td>
<td>2/22/02</td>
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<td>Sequential Automatic Test-Pattern Generation</td>
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<td>Memory Testing</td>
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<td>Analog Testing</td>
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<td>12 &amp; 13</td>
<td>Agrawal/Bushnell</td>
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<td>Built-In Self-Testing I</td>
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<td>4/19/02</td>
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<td>Boundary Scan &amp; Mixed-Signal Test Bus</td>
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<td>5/3/02</td>
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GRADING:

Homeworks 1-13 (Only 10 best are included) 25%
20 Min. In-Class Presentation 10%
Final Paper 15%
Course Project 30%
Final Examination 20%
Total 100%

Note that if you do not interact with the rest of the class during the term, then your In-Class Presentation grade will be reduced.

HOMEWORK AND FINAL EXAM TOPICS:

1. *Homework 1*: Test Introduction and ATE
2. *Homework 2*: Test Economics and Fault Modeling
3. *Homework 3*: Logic and Fault Simulation
4. *Homework 4*: Testability Measures
5. *Homework 5*: Combinational ATPG
6. *Homework 6*: Sequential ATPG
7. *Homework 7*: Memory Testing
8. *Homework 8*: Analog Testing
10. *Homework 10*: Design for Testability
11. *Homework 11*: Built-In Self-Testing
12. *Homework 12*: Boundary Scan and Analog Test Bus
13. *Homework 13*: System Test and CORE-Based Design
14. *Final Exam*: All Topics