18

A Simplistic Approach to the Analysis of Transistor Amplifiers

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18.1 Introduction

The traditional approach to the small-signal analysis of transistor amplifiers employs the transistor models with dependent sources, illustrated in Figure 18.1, for both the MOS and BJT devices. AQ1

In this chapter, techniques for the analysis of transistor circuits will be demonstrated without the use of a small-signal equivalent circuit containing dependent sources. Because of the similarities inherent in the two circuit configurations shown in Figure 18.1, the following analyses will address both MOS and BJT devices in unison.

As a general rule, the small signal parameters are calculated as a function of the transistor currents. In view of that fact, consider now each type of device.

18.1.1 MOS Transistor

In this case:

$$r_m = \frac{1}{g_m} = \frac{1}{\sqrt{2I_D K}} \tag{18.1}$$

where I_D is the drain biasing current

$$K = \mu C_{ox} \frac{W}{L} = K' \frac{W}{L} \tag{18.2}$$

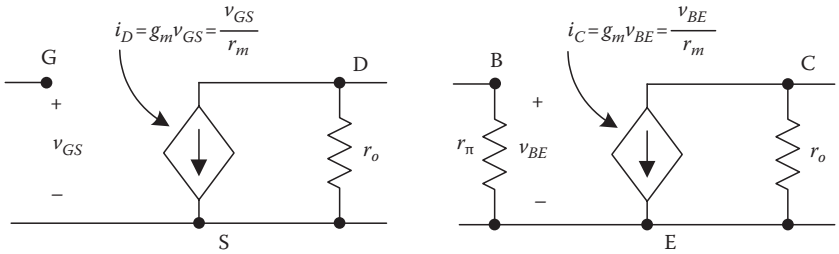


FIGURE 18.1 AQ2

where

K is the transconductance parameter for a specific transistor with channel length L and channel width W

K' is a parameter that characterizes the fabrication process and is the same for all transistors in the circuit

The output resistance is given by the expression:

$$r_o = \frac{(1/\lambda) + V_{DS}}{I_D} \approx \frac{1}{\lambda I_D} \tag{18.3}$$

where the λ parameter describes the slope of the transistor output characteristics.

18.1.2 Bipolar Transistors

In this case,

$$r_m = \frac{1}{g_m} = \frac{V_T}{I_C} \tag{18.4}$$

and

$$r_\pi = (\beta + 1) r_m \tag{18.5}$$

where

I_C is the collector biasing current

V_T is the thermal potential that is equal to about 25 mV at room temperature, as indicated by the expression

$$V_T = \frac{kT}{q} \approx 25 \text{ mV} \tag{18.6}$$

The output resistance is

$$r_o = \frac{V_A + |V_{CE}|}{I_C} \approx \frac{V_A}{I_C} \tag{18.7}$$

where V_A represents the Early voltage that characterizes the slope of the bipolar transistor's output characteristics.

18.2 Calculating Biasing Currents

With MOS transistors, it is assumed that the device operates in the current saturation region. In this region, where $V_{DS} > V_{GS} - V_{th}$, the drain current is given by the expression

$$I_D = \frac{K}{2}\Delta^2 = \frac{K'}{2}\frac{W}{L}\Delta^2 \tag{18.8}$$

where "Δ" = $V_{GS} - V_{th}$ indicates the amount by which the control voltage V_{GS} exceeds the threshold voltage V_{th}.

Example 18.1

Consider the following circuit with the specified parameters (Figure 18.2).

Assuming the gate current is negligible, the gate voltage can be determined from the voltage divider consisting of the resistors R_1 and R_2. Thus, V_G can be calculated as AQ3

$$V_G = \frac{R_2}{R_1 + R_2} V_{DD} = 1\,\text{V} \tag{18.9}$$

$$K = K'\frac{W}{L} = 1\,\text{mA/V}^2 \tag{18.10}$$

$$\Delta = V_{GS} - V_{th} = V_G - V_S - V_{th} = 0.4\,\text{V} \tag{18.11}$$

Therefore the biasing drain current is

$$I_D = \frac{K}{2}\Delta^2 = 80\,\mu\text{A} \tag{18.12}$$

When the MOS transistor has a series resistor, R_S, connected to the source, determination of the biasing drain current is slightly more complicated. Therefore, this situation is analyzed in Example 18.2.

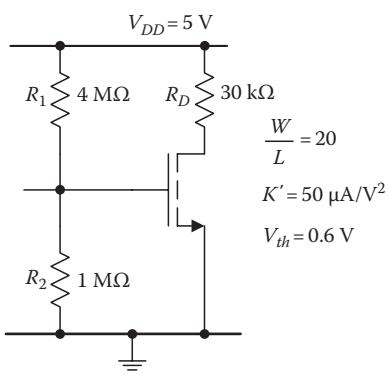


FIGURE 18.2

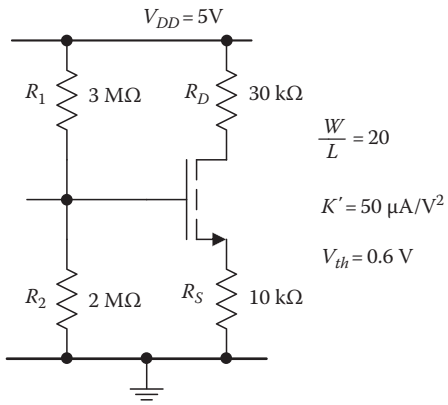


FIGURE 18.3

Example 18.2

The primary difference between this case and the previous one is the presence of R_S (Figure 18.3).

Once again, using the voltage divider consisting of R_1 and R_2, the gate voltage V_G can be found from the expression

$$V_G = \frac{R_2}{R_1 + R_2} V_{DD} = 2\,\text{V} \tag{18.13}$$

$$K = K' \frac{W}{L} = 1\text{mA/V}^2 \tag{18.14}$$

and by definition

$$\Delta = V_{GS} - V_{th} = V_G - V_S - V_{th} \tag{18.15}$$

Employing Ohm's law and using (18.8) yields

$$V_S = I_D R_S = \frac{K}{2} \Delta^2 R_S \tag{18.16}$$

Combining Equations 18.15 and 18.16 produces

$$\Delta = V_G - \frac{K}{2} \Delta^2 R_S - V_{th} \tag{18.17}$$

which can be written as

$$\frac{KR_S}{2} \Delta^2 + \Delta - \left(V_G - V_{th}\right) = 0 \tag{18.18}$$

This is a quadratic equation, the solution of which is

$$\Delta = \frac{-1 \pm \sqrt{1 + 2KR_S\left(V_G - V_{th}\right)}}{KR_S} \tag{18.19}$$

Since Δ must be positive, then

$$\Delta = \frac{1}{KR_S}\left(\sqrt{1+2KR_S\left(V_G - V_{th}\right)} - 1\right) = \frac{1}{10}\left(\sqrt{1+2\cdot 10(1.4)} - 1\right) = 0.43385\ \text{V} \tag{18.20}$$

and thus the drain current is

$$I_D = \frac{K}{2}\Delta^2 = 96.615\ \mu\text{A} \quad \text{or} \quad I_D = \frac{V_G - \Delta - V_{th}}{R_S} = 96.615\ \mu\text{A} \tag{18.21}$$

Other methods could be used to solve the quadratic equation; e.g., I_D or V_S could serve as unknowns. However, in these cases, it would be difficult to decide which root is the correct answer. This problem does not arise when Δ is selected as the unknown.

Consider now determining the biasing currents for BJTs. In this case, a different tack is needed and will be demonstrated in Example 18.3. The following assumptions are usually made:

$$V_{BE} \approx 0.7\ \text{V} \tag{18.22}$$

$$I_C = \beta I_B \tag{18.23}$$

$$I_E \approx I_C \tag{18.24}$$

Example 18.3

A BJT common-emitter circuit is shown in Figure 18.4, together with the transistor parameters.

First of all, it is assumed that the base current is negligible and the base voltage V_B can be determined using the voltage divider consisting of R_1 and R_2. This assumption yields the following voltages and currents:

$$V_B = \frac{R_2}{R_1 + R_2}V_{CC} = 3\ \text{V} \tag{18.25}$$

$$V_E = V_B - V_{BE} = 3 - 0.7 = 2.3 \tag{18.26}$$

$$I_C \approx I_E = \frac{V_E}{R_E} = \frac{V_B - 0.7}{R_E} = 1\text{mA} \tag{18.27}$$

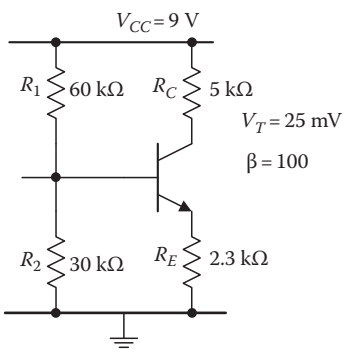


FIGURE 18.4

It is important to note that with this approximate approach, the current gain β is not needed. In situations where this approximation does not hold, i.e., the base current cannot be neglected, then the resistor divider of Figure 18.4 must be replaced by the Thevenin equivalent circuit, shown in Figure 18.5, where

$$R_{TH} = R_1 \| R = \frac{R_1 R_2}{R_1 + R_2} \quad \text{and} \quad V_{TH} = \frac{R_2}{R_1 + R_2}V_{CC} \tag{18.28}$$

Applying Kirchhoff's voltage law to the circuit in Figure 18.5 yields the equation

$$V_{TH} = R_{TH}I_B + V_{BE} + I_E R_E \tag{18.29}$$

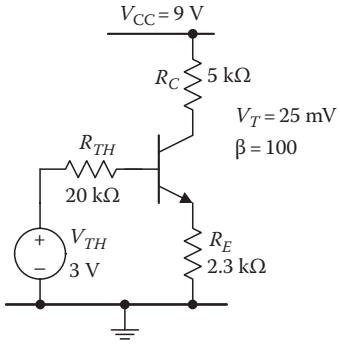


FIGURE 18.5

AQ4 Using Equations 18.22 through 18.24, Equation 18.29 can be rewritten as

$$I_C = \frac{V_{TH} - 0.7}{(R_{TH}/\beta) + R_E} = 0.92\,\text{mA} \tag{18.30}$$

18.3 Small Signal Analysis

Given the transistor currents, the small signal parameters r_m and r_o can be determined using Equations 18.1 and 18. 3 for MOS transistors and Equations 18.4 and 18.7 for bipolar transistors. MOS transistors can operate in one of three configurations: CS—common source, CD—common drain, and CG—common gate. In a similar manner, bipolar transistors operate in one of the following three configurations: CE—common emitter, CC—common collector, and CB—common base. These different configurations will now be analyzed.

18.3.1 Common-Source and Common-Emitter Configurations

Figure 18.6 illustrates a transistor in the common-emitter configuration. The biasing current for this structure was determined in Example 18.3. An inspection of the circuit indicates that the incremental collector/emitter current Δi_C can be found from Ohm's law as

$$\Delta i_C = \frac{\Delta v_{in}}{r_m + R_E} \tag{18.30}$$

Furthermore, this incremental current, Δi_C, will create an incremental output voltage of

$$\Delta v_{out} = -\Delta i_C R_C \tag{18.31}$$

Substituting Equation 18.30 into Equation 18.31 yields

$$\Delta v_{out} = -\Delta v_{in} \frac{R_C}{r_m + R_E} \tag{18.32}$$

Therefore, the voltage gain of this single stage amplifier is

$$A_V = \frac{\Delta v_{out}}{\Delta v_{in}} = -\frac{R_C}{r_m + R_E} \tag{18.33}$$

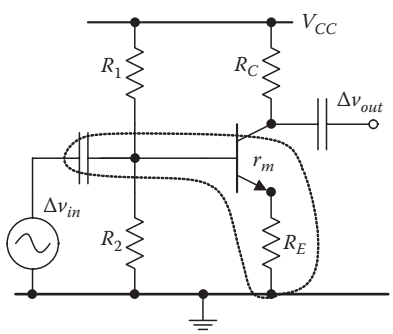


FIGURE 18.6

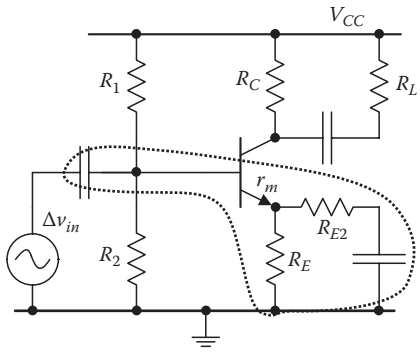


FIGURE 18.7

It the transistor circuit of Figure 18.6 is modified to contain the additional elements shown in Figure 18.7, then Equation 18.30 must be modified as follows:

$$\Delta i_C = \frac{\Delta v_{in}}{r_m + R_E \,||\, R_{E2}} \tag{18.34}$$

and the effective load resistance would be the parallel combination of R_C and R_L. As a consequence, the new form for Equation 18.31 is

$$\Delta v_{out} = -\Delta i_C \left(R_C \,||\, R_L \right) \tag{18.35}$$

and the transistor voltage gain is

$$A_V = \frac{\Delta v_{out}}{\Delta v_{in}} = -\frac{R_C \,||\, R_L}{r_m + R_E \,||\, R_{E2}} \tag{18.36}$$

At this point, it is important to note that the traditional lengthy derivation of the gain, which employs the transistor model with a dependent current source as shown in Figure 18.1b, yields the voltage gain A_V:

$$A_V = -\frac{g_m \left(R_C R_L / R_C + R_L \right)}{1 + g_m \left(R_E R_{E2} / R_E + R_{E2} \right)} \tag{18.37}$$

which is, of course, the same as Equation 18.36. If circuit configuration has an additional series base resistance, R_B, then Equation 18.36 should be rewritten as

$$\Delta i_C = \frac{\Delta v_{in}}{(R_B / \beta) + r_m + R_E \,||\, R_{E2}} \tag{18.38}$$

and then

$$A_V = \frac{\Delta v_{out}}{\Delta v_{in}} = -\frac{R_C \,||\, R_L}{(R_B / \beta) + r_m + R_E \,||\, R_{E2}} \tag{18.39}$$

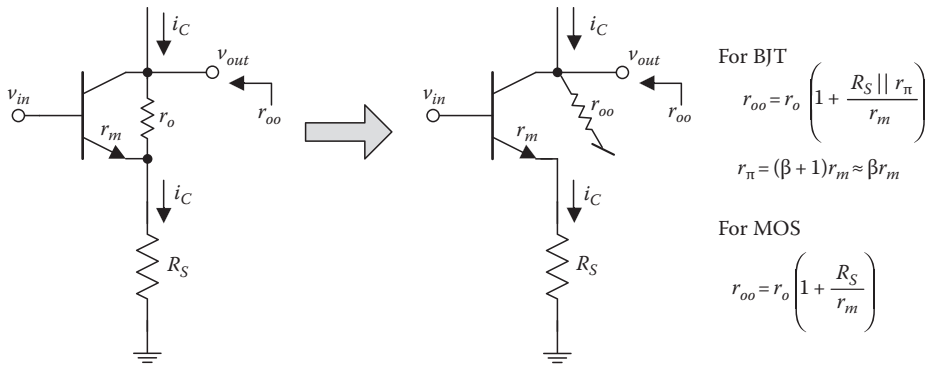


FIGURE 18.8

In the foregoing analysis, the transistor output resistance r_{oo} was ignored. If this output resistance should be included in the calculations, then Equation 18.36 must be slightly modified to include it as follows:

$$A_V = \frac{\Delta v_{out}}{\Delta v_{in}} = -\frac{R_C \,||\, R_L \,||\, r_{oo}}{r_m + R_E \,||\, R_{E2}} \tag{18.40}$$

The calculation of r_{oo} is relatively complicated and requires the use of the traditional small signal analysis using dependent sources. Figure 18.8 provides the results of this analysis in which slightly different equations must be used for bipolar and MOS transistors. The output resistance of the BJT with R_S connected to its emitter is

$$r_{oo} = r_o + \frac{r_o\left(R_S \,||\, r_\pi\right)}{r_m} + R_S \,||\, r_\pi \approx r_o\left(1 + \frac{R_S \,||\, r_\pi}{r_m}\right) \tag{18.41}$$

where $r_\pi = (\beta + 1)r_m$. In this case, the MOS transistor can be considered as a BJT with $r_\pi = \infty$ and thus

$$r_{oo} = r_o + \frac{r_o R_S}{r_m} + R_S \approx r_o\left(1 + \frac{R_S}{r_m}\right) \tag{18.42}$$

Calculation of an amplifier's input and output resistances are also an important part of small signal analysis. The circuit in Figure 18.6 indicates that the input resistance is

$$r_{in} = R_1 \,||\, R_2 \,||\left(\beta\left(r_m + R_E\right)\right) \tag{18.43}$$

Note that the assumption that $\beta + 1 \approx \beta$ is consistently employed to simplify the equations. This assumption is based upon the fact that there is no good reason to use $\beta + 1$ because the actual value of β is never really known, and furthermore, β fluctuates with temperature (about 1% per °C). Thus, an analysis of the circuit in Figure 18.7 indicates that

$$r_{in} = R_1 \,||\, R_2 \,||\left(\beta\left(r_m + R_E \,||\, R_{E2}\right)\right) \tag{18.44}$$

Clearly, if the BJT in Figure 18.6 or Figure 18.7 is replaced by a MOS device ($\beta = \infty$), then the input resistance would simply be

$$r_{in} = R_1 \,||\, R_2 \tag{18.45}$$

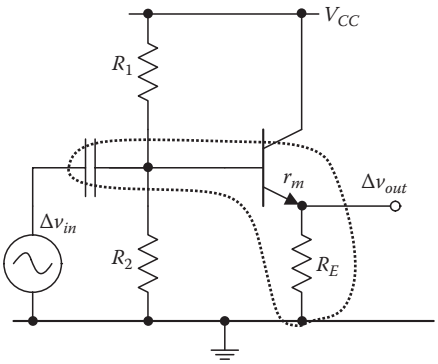


FIGURE 18.9

18.3.2 Common-Drain and Common-Collector Configurations

Figure 18.9 illustrates a BJT in the common-collector configuration. An inspection of this circuit indicates that the incremental collector/emitter current Δi_C is

$$\Delta i_C = \frac{\Delta v_{in}}{r_m + R_E} \tag{18.46}$$

and the output voltage is

$$\Delta v_{out} = \Delta i_C R_E \tag{18.47}$$

Therefore, the voltage gain is

$$A_V = \frac{\Delta v_{out}}{\Delta v_{in}} = \frac{R_E}{R_E + r_m} \tag{18.48}$$

Note carefully that Equation 18.48 is simply the equation for a voltage divider with resistors R_E and r_m:

In the event that a base resistance is present, as shown in Figure 18.10, then using Kirchhoff voltage law:

$$\Delta v_{in} = R_B \Delta i_B + (r_m + R_E)\Delta i_C = \left[\frac{R_B}{\beta} + (r_m + R_E)\right]\Delta i_C \tag{18.49}$$

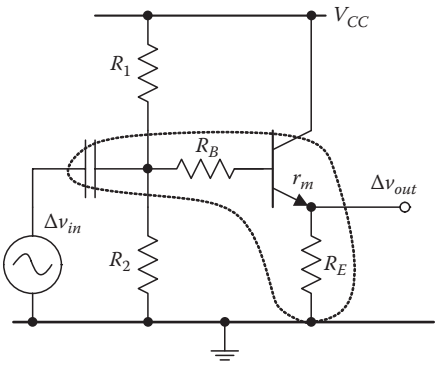


FIGURE 18.10

and thus

$$\Delta i_C = \frac{\Delta v_{in}}{(R_B/\beta) + r_m + R_E} \tag{18.50}$$

$$\Delta v_{out} = \Delta i_C R_E \tag{18.51}$$

and once again, the voltage gain is determined from the resistor divider equation

$$A_V = \frac{\Delta v_{out}}{\Delta v_{in}} = \frac{R_E}{(R_B/\beta) + r_m + R_E} \tag{18.52}$$

18.3.3 Common-Gate and Common-Base Configurations

Figure 18.11 is an illustration of a transistor in the common-collector configuration. Note that in this case, the incremental collector/emitter current Δi_C is

$$\Delta i_C = \frac{\Delta v_{in}}{r_m} \tag{18.53}$$

The small signal analysis for this situation ignores the resistor R_E since it is connected in parallel with the ideal voltage source. The voltage drop across resistor R_C is

$$\Delta v_{out} = \Delta i_C R_C \tag{18.54}$$

and thus the voltage gain is the ratio of two resistors:

$$A_V = \frac{\Delta v_{out}}{\Delta v_{in}} = \frac{R_C}{r_m} \tag{18.55}$$

The addition of a base resistor, as indicated in Figure 18.12, makes the circuit slightly more complicated, and in this case, Equation 18.55 must be modified to include this R_B resistor. The resulting equation is

$$A_V = \frac{\Delta v_{out}}{\Delta v_{in}} = \frac{R_C}{r_m + (R_B/\beta)} \tag{18.56}$$

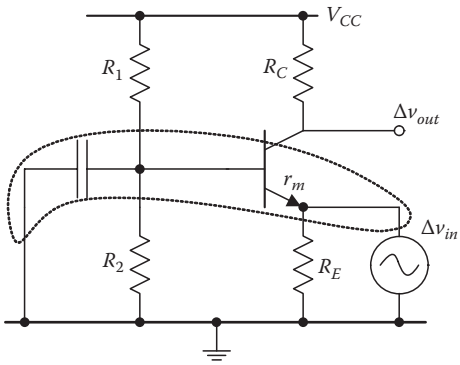


FIGURE 18.11

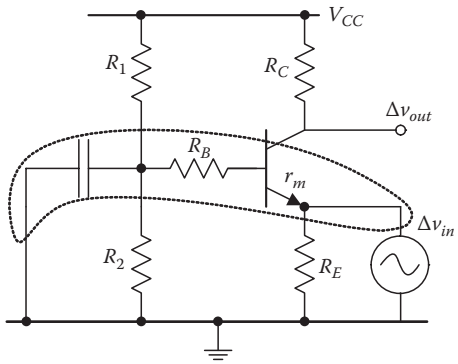


FIGURE 18.12

Note that voltage drop across R_B is $\Delta v_{RB} = i_B R_B$ and since $i_C = \beta i_B$ then $\Delta v_{RB} = i_C R_B/\beta$. The voltage drop across r_m is $i_C r_m$. Since the denominator in Equation 18.56 represents the sum of these two voltage drops, Equation 18.56 indicates that the voltage gain is also equal to the ratio of two resistors.

In a small signal analysis, MOS transistors and BJTs are treated basically the same, even though their small signal parameters r_m and r_o are calculated differently. One may also treat a MOS transistor as a BJT with a current gain $\beta = \infty$

Example 18.4

Consider now the use of the proposed method for the same circuits that were analyzed in a classical way in the previous chapter entitled "Transistors in amplifier circuits." Figure 3.12 in that chapter is repeated in Figure 18.13.

An inspection of the circuit indicates that

$$r_{in} = R_1 \| R_2 = \frac{R_1 R_2}{R_1 + R_2} \tag{18.57}$$

where r_{in} is the parallel combination of the two biasing resistors R_1 and R_2. In the MOS transistor case, its input resistance can be neglected. The output resistance is again a parallel combination of R_D and r_o

$$r_{out} = R_D \| r_o = \frac{R_D r_o}{R_D + r_o} \tag{18.58}$$

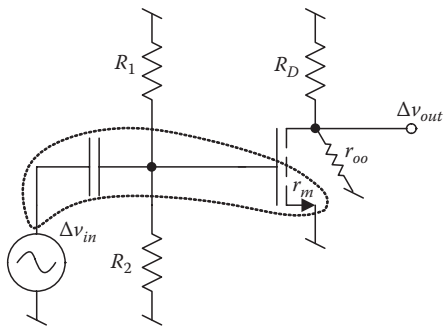


FIGURE 18.13

The gain of the amplifier is then the ratio of the output resistance to r_m, provided that there is no series resistance connected to the source:

$$A_V = -\frac{R_D \,||\, r_o}{r_m} \tag{18.59}$$

This same result would require several pages of analysis using the traditional approach.

Example 18.5

Consider now the circuit shown in Figure 18.14a, which is identical to the one in Figure 3.16 in the previous chapter. The amplifier gain, and the input and output resistances can be found using the approach presented here. In this case, the amplifier gain is

$$A_V = \frac{-R_C \,||\, R_L \,||\, r_{oo}}{r_m + R_E} \tag{18.60}$$

where r_{oo} is given by Equation 18.42, in which R_S is replaced with R_E.

The traditional approach, outlined in the previous chapter where the effect of r_o was ignored, yielded the gain equation

$$A_V = \frac{-g_m(R_C \,||\, R_L)}{1 + R_E\left((1/r_\pi) + g_m\right)} \tag{18.61}$$

With the substitutions $g_m = 1/r_m$ and $r_\pi = \beta\, r_m$ the gain becomes

$$A_V = \frac{-R_C \,||\, R_L}{r_m\left(1 + R_E\left((1/\beta r_m) + (1/r_m)\right)\right)} = \frac{-R_C \,||\, R_L}{\left(r_m + R_E\left((1/\beta) + 1\right)\right)} \approx \frac{-R_C \,||\, R_L}{r_m + R_E} \tag{18.62}$$

The input resistance of r_{in} of the circuit shown in Figure 18.14a represents the parallel combination of the two biasing resistors R_1, R_2 and $\beta(r_m + R_E)$

$$r_{in} = R_1 \,||\, R_2 \,||\, \beta\left(r_m + R_E\right) \tag{18.63}$$

The output resistance is the parallel combination of R_C, R_L, and r_{oo}

$$r_{out} = R_C \,||\, R_L \,||\, r_{oo} = R_C \,||\, R_L \,||\left(r_o\left(1 + \frac{R_E \,||\left(r_m\beta\right)}{r_m}\right)\right) \tag{18.64}$$

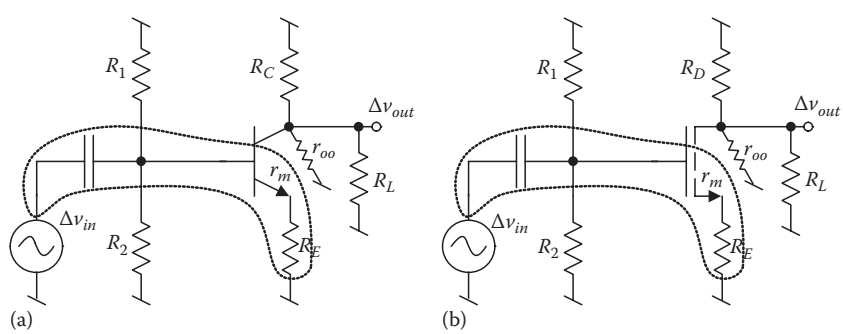


FIGURE 18.14

In the MOS transistor case (Figure 18.14b), the input resistance of the transistor can be neglected, and the output resistance is once again a parallel combination of R_D, R_L, and r_{oo}, so

$$r_{in} = R_1 \| R_2 \tag{18.65}$$

The output resistance is the parallel combination of R_C, R_L, and r_{oo}

$$r_{out} = R_D \| R_L \| r_{oo} = R_D \| R_L \| \left(r_o \left(1 + \frac{R_S}{r_m} \right) \right) \tag{18.66}$$

18.4 Circuits with PNP and PMOS Transistors

Circuits with PNP and PMOS transistors can be handled in a manner similar to that employed for circuits with NPN and NMOS transistors. In order to avoid confusion, the best approach is the use of mirrored circuits, as shown in Figure 18.15. Note that the mirror image circuit is exactly the same as the original one, but simply drawn differently. In the mirror image circuit, the reference voltage is changed so that the bottom node is at 0 V potential and the top node is at −8 V potential. With this configuration, the dc analysis for the mirror image circuit is now essentially identical to that of the NPN transistor in Example 18.3. The approximate solution for this case yields

$$V_B = \frac{4\ \text{k}\Omega}{4\ \text{k}\Omega + 14\ \text{k}\Omega}\left(-9\ \text{V}\right) = 2\ \text{V} \tag{18.67}$$

$$V_E = V_B - V_{BE} = -2 - (-0.7) = -1.3\ \text{V} \tag{18.68}$$

$$I_C \approx I_E = \frac{V_E}{R_E} = \frac{-1.3\ \text{V}}{1.3\ \text{k}\Omega} = -1\ \text{mA} \tag{18.69}$$

With the more accurate approach, the resistor divider consisting of the 4 and 12 kΩ resistors must be replaced by a Thevenin equivalent circuit in which

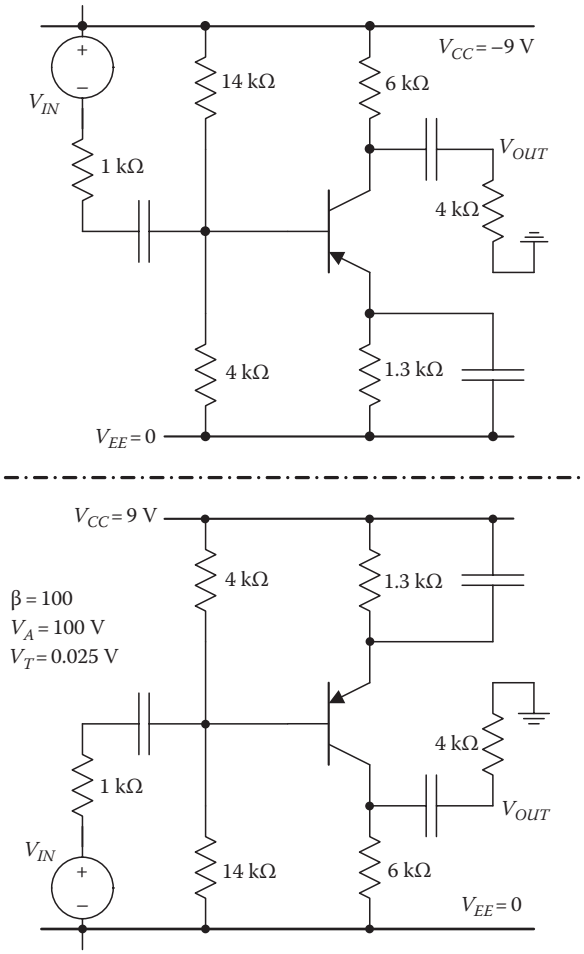
$$R_{TH} = 4\ \text{k}\Omega \| 14\ \text{k}\Omega = \frac{4\ \text{k}\Omega \cdot 14\ \text{k}\Omega}{4\ \text{k}\Omega + 14\ \text{k}\Omega} = 3.111\ \text{k}\Omega \quad \text{and} \quad V_{TH} = \frac{4\ \text{k}\Omega}{4\ \text{k}\Omega + 14\ \text{k}\Omega}\left(-9\ \text{V}\right) = 2\ \text{V} \tag{18.70}$$

Now the accurate value of current can be determined as

$$I_C = \frac{V_{TH} - 0.7}{(R_{TH}/\beta) + R_E} = \frac{2 - 0.7}{(3.111\ \text{k}\Omega/100) + 1.3\ \text{k}\Omega} = 0.977\ \text{mA} \tag{18.71}$$

If the mirror image circuit, shown in Figure 18.16, is used, the small signal analysis can also be used in a manner similar to that employed for NPN transistors. First, the small signal parameters are calculated as

$$r_m = \frac{V_T}{I_C} = \frac{25\ \text{mV}}{1\ \text{mA}} = 25\ \Omega \tag{18.72}$$



AQ5 **FIGURE 18.15**

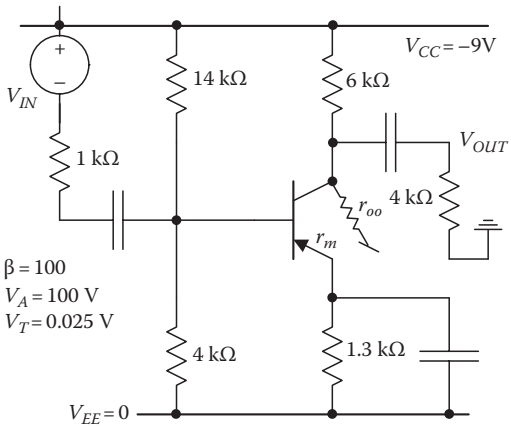


FIGURE 18.16

$$r_o = \frac{V_A}{I_C} = \frac{100\text{ V}}{1\text{ mA}} = 100\text{ k}\Omega \tag{18.73}$$

Then, the input and load resistances are computed. The input resistance, as seen by input capacitor, is

$$r_{IN} = 14\text{ k}\Omega \,||\, 4\text{ k}\Omega \,||\, (\beta \cdot r_m) = 14\text{ k}\Omega \,||\, 4\text{ k}\Omega \,||\, 2.5\text{ k}\Omega = 1.386\text{ k}\Omega \tag{18.74}$$

Because the emitter of the PNP transistor is grounded, $r_{oo} = r_o$. The load resistance, i.e., the resistance between the collector and ground, is

$$r_L = 6\text{ k}\Omega \,||\, 4\text{ k}\Omega \,||\, r_{oo} = 6\text{ k}\Omega \,||\, 4\text{ k}\Omega \,||\, 100\text{ k}\Omega = 2.344\text{ k}\Omega \tag{18.75}$$

Because of the presence of the 1 kΩ series source resistance, the gain calculation must be done in two steps. First, the gain (loss) from the signal source to the transistor base is calculated using the resistor divider:

$$A_{V1} = \frac{r_{IN}}{r_{IN} + 1\text{ k}\Omega} = \frac{1.386\text{ k}\Omega}{1.386\text{ k}\Omega + 1\text{ k}\Omega} = 0.581 \tag{18.76}$$

The voltage gain of the transistor from base to collector is

$$A_{V2} = \frac{r_L}{r_m} = \frac{2.344\text{ k}\Omega}{25\ \Omega} = 93.76 \tag{18.77}$$

Then, the total circuit gain is

$$A_V = A_{V1}A_{V2} = 0.581 \cdot 93.76 = 54.5 \tag{18.78}$$

18.5 Analysis of Circuits with Multiple Transistors

In integrated circuits, especially MOS technology, it is much easier, and cheaper, to fabricate transistors than resistors. Therefore, a new concept in circuit design was developed resulting in a circuit in which the number of transistors is typically larger than the number of resistors. In addition, in integrated circuits, it is not possible to use large values of capacitance. Figure 18.17 shows how the blocking capacitor can be replaced by an additional transistor. The circuit in Figure 18.17a has the voltage gain of

$$A_V = -\frac{R_D \,||\, r_{oo}}{r_m} \approx -\frac{R_D}{r_m} \tag{18.79}$$

In this case, it is assumed that the signal frequency is large enough so that the capacitor C shorts the resistor R_S. This assumption is, of course, invalid if the signal frequency is lower than $1/R_SC$. In the modified circuit, i.e., Figure 18.17b, the resistance seen by the source is equal to parallel combination of R_S and the r_m of the M2 transistor. Note that circuit of Figure 18.17b also works well at low frequencies. The voltage gain is then

$$A_V = -\frac{R_D \,||\, r_{oo}}{r_{m1} + r_{m2} \,||\, R_S} \approx -\frac{R_D}{2r_m} \tag{18.80}$$

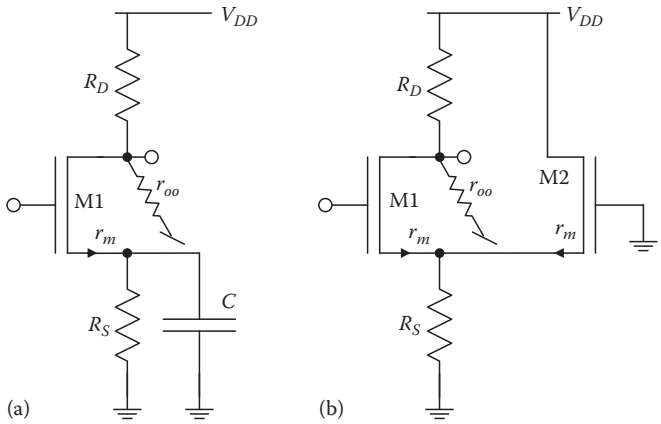


FIGURE 18.17

Proceeding up a notch, consider the circuit shown in Figure 18.18. The voltage gain from the input to the drain of M1 is given by Equation 18.80. The gain calculation from the input to the drain of M2 should be done in two steps. First, the common drain approach is used to calculate the gain from the input to the node associated with the transistor sources:

$$A_{V1} = -\frac{r_{m2} \,||\, R_S}{r_{m1} + r_{m2} \,||\, R_S} \approx 0.5 \tag{18.81}$$

Then, the gain from the source to the drain of M2 is determined using the common gate configuration, which yields

$$A_{V2} = +\frac{R_{D2} \,||\, r_{oo}}{r_{m2}} \approx \frac{R_{D2}}{r_m} \tag{18.82}$$

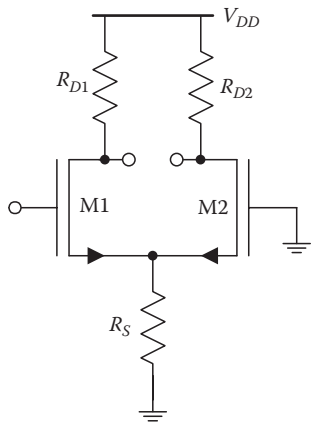


FIGURE 18.18

Finally, the total voltage gain is

$$A_V = A_{V1}A_{V2} = \frac{R_{D2}}{2r_m} \tag{18.83}$$

The next example is an analysis of a simple amplifier with a current mirror as shown in Figure 18.19. The current mirror is composed of the transistors M3 and M4, and it is assumed that current i_3 is equal to current i_1. A popular technique used to analyze the differential amplifier employs the assumption that half of the input voltage is applied at input 1 and another half, with opposite sign, is applied at input 2. This voltage on the nodes associated with the sources of M1 and M2 is not changing and is considered to be a virtual ground. Therefore, the input 1 signal, which is equal to $0.5v_{in}$, drives r_{m1}:

$$\Delta i_1 = \frac{0.5\Delta v_{in}}{r_{m1}} \tag{18.84}$$

and the other half of the input signal, with opposite sign, drives r_{m2}:

$$\Delta i_2 = -\frac{0.5\Delta v_{in}}{r_{m2}} \tag{18.85}$$

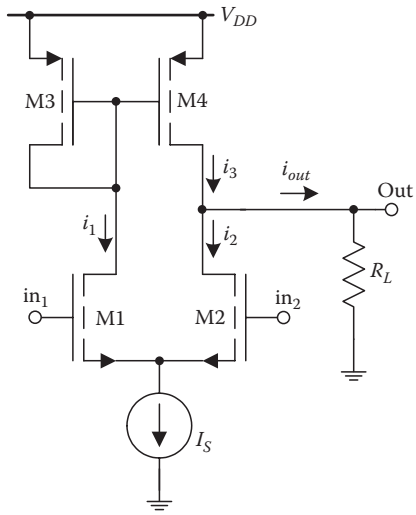


FIGURE 18.19

Since $i_3 = i_1$, then

$$\Delta i_{out} = \Delta i_3 - \Delta i_2 = \Delta i_1 - \Delta i_2 = 0.5\Delta v_{in}\left(\frac{1}{r_{m1}} + \frac{1}{r_{m2}}\right) = \frac{\Delta v_{in}}{r_m} \tag{18.86}$$

and the incremental output voltage is

$$\Delta v_{out} = \Delta i_{out} R_L = \frac{R_L}{r_m}\Delta v_{in} \tag{18.87}$$

Hence, the voltage gain is

$$A_v = \frac{\Delta v_{out}}{\Delta v_{in}} = \frac{R_L}{r_m} \tag{18.88}$$

If the output resistance, r_o, of each transistor must be considered, then these resistances should be connected in parallel with the loading resistor R_L. Under this condition,

$$A_v = \frac{\Delta v_{out}}{\Delta v_{in}} = \frac{R_L \,||\, r_{oP} \,||\, r_{oN}}{r_m} \tag{18.89}$$

The next example considers the analysis of the two-stage amplifier shown in Figure 18.20. Assuming all transistors are the same size, one finds that the drain currents of transistors M5, M6, M7, and M8 are equal to I_S. In addition, the drain currents of transistors M1, M2, M3, and M4 are equal to $0.5I_S$, assuming an equal division of biasing currents between M1 and M2. From this knowledge of the transistor currents, the small signal parameters, r_m and r_o, can be found using Equations 18.1 and 18.3. An inspection of this circuit, and use of Equation 18.87, yields the voltage gain of the first stage as

$$A_{v1} = \frac{r_{oP} \,||\, r_{oN}}{r_m} = \frac{r_{o4} \,||\, r_{o2}}{r_m} \tag{18.90}$$

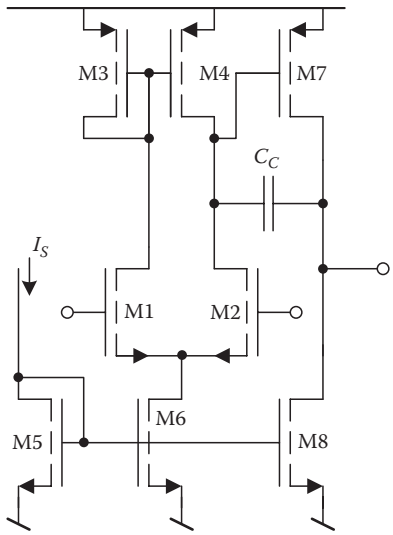


FIGURE 18.20

Note that in this stage there is no R_L. In addition, it is assumed that the source current was equally divided and $r_{m1} = r_{m2} = r_m$.

The second stage of the circuit in Figure 18.20 is the common source amplifier consisting of transistor M7 with transistor M8 acting as the load. Therefore, the voltage gain of the second stage is

$$A_{v2} = \frac{r_{o7} \,||\, r_{o8}}{r_{m7}} \tag{18.91}$$

The total voltage gain is

$$A_v = A_{v1}A_{v2} = \frac{r_{o4} \,||\, r_{o2}}{r_{m1}} \frac{r_{o7} \,||\, r_{o8}}{r_{m7}} \tag{18.92}$$

If this circuit is considered to be a transconductance amplifier, then the transconductance parameter, G_m, is

$$G_m = \frac{r_{o4} \,||\, r_{o2}}{r_{m1}} \frac{1}{r_{m7}} \tag{18.93}$$

and the output resistance of the circuit is

$$R_{out} = r_{o7} \,||\, r_{o8} \tag{18.94}$$

Obviously, for MOS input stages, the input resistance is $R_{in} = \infty$.

It can be shown that other key parameters of the amplifier of Figure 18.20 can also be found using the simplistic analysis method. For example, the location of the first pole, i.e., the first corner frequency shown in Figure 18.21, is given by the expression

$$\omega_0 = \frac{1}{A_v r_{m1} C_C} = \frac{1}{A_{v1} A_{v2} r_{m1} C_C} \tag{18.95}$$

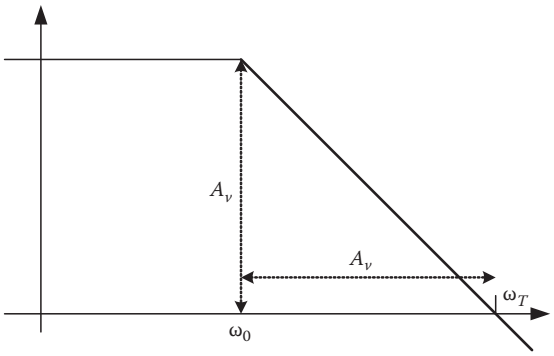


FIGURE 18.21

Then the Gain-Bandwidth product, GB, for the amplifier is equal to the cutoff frequency defined by the time constant $r_{m1}C_C$

$$GB = A_{v1}A_{v2}\omega_0 = \omega_T = \frac{1}{C_C r_{m1}} \tag{18.96}$$

The second pole is located in the high frequency range above ω_T, and it can usually be ignored because the amplifier gain at this frequency is smaller than one. If this is not the case, then the value of C_C should be chosen large enough that the ratio between the second and first pole frequencies is larger than A_V.

The Slew Rate, SR, is dependent upon the speed with which the capacitor C_C can be charged. With the largest possible input voltage difference, the maximum charging current would be the source current of M6 that is approximately equal to I_S. Therefore

$$SR = \frac{I_S}{C_C} \tag{18.97}$$

The circuit in Figure 18.20 has a relatively large output resistance, given by Equation 18.94, and should be considered an Operational Transconductance Amplifier (OTA), rather than an Operational Amplifier (OPAMP). An OTA can be converted into an OPAMP by adding a unity gain buffer to the circuit. This additional element could be a simple voltage follower, as shown in Figure 18.22a, or more advanced push-pull amplifier, as shown in Figure 18.22b.

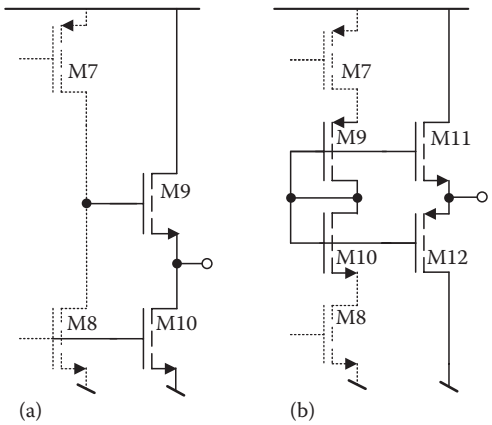


FIGURE 18.22

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