Bipolar Junction Transistor

9.1 Ebers–Moll Model ................................................................. 9-1
9.2 Gummel–Poon Model ........................................................... 9-3
9.3 Current Gains of Bipolar Transistors ..................................... 9-5
9.4 High Current Phenomena ....................................................... 9-7
9.5 Small Signal Model .............................................................. 9-8
9.6 Technologies ........................................................................ 9-10
    Integrated NPN Bipolar Transistor • Lateral and Vertical
    PNP Transistors
9.7 Model Parameters .................................................................. 9-12
    Thermal Sensitivity • Second Order Effects • SPICE Model of the
    Bipolar Transistor
9.8 SiGe HBTs ........................................................................... 9-15
    Operation Principle and Performance Advantages over
    Si BJT • Industry Practice and Fabrication Technology
9.9 References ............................................................................ 9-20

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The bipolar junction transistor (BJT) is historically the first solid-state analog amplifier and digital switch, and formed the basis of integrated circuits (IC) in the 1970s. Starting in the early 1980s, the MOSFET had gradually taken over; particularly for mainstream digital ICs. However, in the 1990s, the invention of silicon–germanium base heterojunction bipolar transistor (SiGe HBT) brought the bipolar transistor back into high-volume commercial production, mainly for the now widespread wireless and wire line communications applications. Today, SiGe HBTs are used to design radio-frequency integrated circuits and systems for cell phones, wireless local area network (WLAN), automobile collision avoidance radar, wireless distribution of cable television, millimeter wave radios, and many more applications, due to its outstanding high-frequency performance and ability to integrate with CMOS for realizing digital, analog, and RF functions on the same chip.

Below, we will first introduce the basic concepts of BJT using a historically important equivalent circuit model, the Ebers–Moll model. Then the Gummel–Poon model will be introduced, as it is widely used for computer-aided design, and is the basis of modern BJT models like the VBIC, Mextram, and HICUM models. Current gain, high current phenomena, fabrication technologies, and SiGe HBTs will then be discussed.

9.1 Ebers–Moll Model

An NPN BJT consists of two closely spaced PN junctions connected back to back sharing the same p-type region, as shown in Figure 9.1a. The drawing is not to scale. The emitter and base layers are thin, typically less than 1 μm, and the collector is much thicker to support a high output voltage swing. For forward mode operation, the emitter–base (EB) junction is forward biased, and the collector-base (CB) junction is reverse biased. Minority carriers are injected from the emitter to base,
travel across the base, and are then collected by the reverse biased CB junction. Therefore, the collector current is transported from the EB junction, and thus is proportional to the EB junction current. In the forward–active mode, the current–voltage characteristic of the EB junction is described by the well-known diode equation

\[
I_E = I_{E0} \left[ \exp \left( \frac{V_{BE}}{V_T} \right) - 1 \right]
\]

where

\( I_{E0} \) is the EB junction saturation current
\( V_T = kT/q \) is the thermal potential (about 25 mV at room temperature)

The collector current is typically smaller than the emitter current is, \( I_{CF} = \alpha_F I_{EF} \), where \( \alpha_F \) is the forward current gain.

Under reverse mode operation, the CB junction is forward biased and the EB junction is reverse biased. Like in the forward mode, the forward biased CB junction current gives the collector current

\[
I_C = I_{C0} \left[ \exp \left( \frac{V_{BC}}{V_T} \right) - 1 \right]
\]

where \( I_{C0} \) is the CB junction saturation current. Similarly \( I_{ER} = \alpha_R I_{IR} \), where \( \alpha_R \) is the reverse current gain. Under general biasing conditions, it can be proven that to first order, a superposition of the above-described forward and reverse mode equivalent circuits can be used to describe the transistor operation, as shown in Figure 9.1b. The forward transistor operation is described by Equation 9.1, and the
Bipolar Junction Transistor

reverse transistor operation is described by Equation 9.2. From the Kirchoff’s current law one can write
$I_C = I_C^R - I_C^E, I_E = I_E^F - I_E^R, and I_R = I_R - I_C$. Using Equations 9.1 and 9.2 the emitter and collector currents can be described as

$$
I_E = a_{11} \left( \exp \frac{V_{RE}}{V_T} - 1 \right) - a_{12} \left( \exp \frac{V_{RC}}{V_T} - 1 \right)
$$

$$
I_C = a_{21} \left( \exp \frac{V_{RE}}{V_T} - 1 \right) - a_{22} \left( \exp \frac{V_{RC}}{V_T} - 1 \right)
$$

(9.3)

which are known as the Ebers–Moll equations [1]. The Ebers–Moll coefficients $a_{ij}$ are given as

$$
a_{11} = I_{E0}, a_{12} = \alpha F I_{C0}, a_{21} = \alpha F I_{E0}, a_{22} = I_{C0}
$$

(9.4)

The Ebers–Moll coefficients are a very strong function of the temperature

$$
a_{ij} = K_i T^m \exp \frac{V_{go}}{V_T}
$$

(9.5)

where

$K_i$ is proportional to the junction area and is independent of the temperature

$V_{go} = 1.21$ V is the bandgap voltage in silicon (extrapolated to 0 K)

$m$ is a material constant with a value between 2.5 and 4

When both EB and CB junctions are forward biased, the transistor is called to be working in the saturation region. Current injection through the collector junction may activate the parasitic transistors in integrated circuits by using a p-type substrate, where the base acts as the emitter, the collector as the base, and the substrate as the collector. In typical integrated circuits, bipolar transistors must not operate in saturation. Therefore, for the integrated bipolar transistor the Ebers–Moll equations can be simplified to the form

$$
I_E = a_{11} \left( \exp \frac{V_{RE}}{V_T} - 1 \right)
$$

$$
I_C = a_{21} \left( \exp \frac{V_{RE}}{V_T} - 1 \right)
$$

(9.6)

where $a_{21}/a_{11} = \alpha F$. This equation corresponds to the circuit diagram shown in Figure 9.1.c.

9.2 Gummel–Poon Model

In real bipolar transistors, the current voltage characteristics are more complex than those described by the Ebers–Moll equations. Typical current–voltage characteristics of the bipolar transistor, plotted in semi-logarithmic scale, are shown in Figure 9.2. At small-base emitter voltages, due to the generation–recombination phenomena, the base current is proportional to

$$
I_{BL} \approx \exp \frac{V_{RE}}{2V_T}
$$

(9.7)
Also, due to the base conductivity modulation at high-level injections, the collector current for larger voltages can be expressed by the similar relation

$$I_C \propto \exp \left( \frac{V_{BE}}{2V_T} \right)$$

(9.8)

Note, that the collector current for a wide range is given by

$$I_C = I_s \exp \left( \frac{V_{BE}}{V_T} \right)$$

(9.9)

The saturation current is a function of device structure parameters

$$I_s = \frac{qA_0n_iV_T\mu_B}{\int_0^{w_B} N_B(x)dx}$$

(9.10)

where

- \( q = 1.6 \times 10^{-19} \) C is the electron charge
- \( A \) is the emitter–base junction area
- \( n_i \) is the intrinsic concentration (\( n_i = 1.5 \times 10^{10} \) at 300 K)
- \( \mu_B \) is the mobility of the majority carriers in the transistor base
- \( w_B \) is the effective base thickness
- \( N_B(x) \) is the distribution of impurities in the base

Note, that the saturation current is inversely proportional to the total impurity dose in the base. In the transistor with the uniform base, the saturation current is given by

$$I_s = \frac{qA_0n_iV_T\mu_B}{w_B N_B}$$

(9.11)
Bipolar Junction Transistor

When a transistor operates in the reverse-active mode (emitter and collector are switched), then the current of such a biased transistor is given by

\[ I_R = I_s \exp \frac{V_{BE}}{V_T} \]  

(9.12)

Note, that the \( I_s \) parameter is the same for forward and reverse modes of operation. The Gummel–Poon transistor model \[2\] was derived from the Ebers–Moll model using the assumption that \( a_{12} = a_{21} = I_c \). For the Gummel–Poon model, Equations 9.3 are simplified to the form

\[ I_R = I_s \left( \frac{1}{\alpha_F} \exp \frac{V_{BE}}{V_T} - \exp \frac{V_{BE}}{V_T} \right) \]  

(9.13)

\[ I_C = I_s \left( \frac{\exp V_{BE} - 1}{\alpha_R} \exp \frac{V_{BC}}{V_T} \right) \]

Those equations require only three coefficients, while the Ebers–Moll requires four. The saturation current \( I_s \) is constant for a wide range of currents. The current gain coefficients \( \alpha_F \) and \( \alpha_R \) have values smaller, but close to unity. Often instead of using the current gain as \( \alpha = I_c/I_s \), the current gain \( \beta \) as a ratio of the collector current to the base current \( \beta = I_C/I_B \) is used. The mutual relationships between \( \alpha \) and \( \beta \) coefficients are given by

\[ \alpha_F = \frac{\beta_R}{\beta_F + 1} \quad \beta_F = \frac{\alpha_F}{1 - \alpha_F} \quad \alpha_R = \frac{\beta_R}{\beta_R + 1} \quad \beta_R = \frac{\alpha_R}{1 - \alpha_R} \]  

(9.14)

The Gummel–Poon model was implemented in SPICE \[3\] and other computer programs for circuit analysis. To make the equations more general, the material parameters \( \eta_F \) and \( \eta_R \) were introduced:

\[ I_C = I_s \left[ \frac{\exp V_{BE}}{\eta_F V_T} - \left( 1 + \frac{1}{\eta_R} \right) \exp \frac{V_{BC}}{\eta_R V_T} \right] \]  

(9.15)

The values of \( \eta_F \) and \( \eta_R \) vary from one to two.

9.3 Current Gains of Bipolar Transistors

The transistor current gain \( \beta \), is limited by two phenomena: base transport efficiency and emitter injection efficiency. The effective current gain \( \beta \) can be expressed as

\[ \frac{1}{\beta} = \frac{1}{\beta_F} + \frac{1}{\beta_T} + \frac{1}{\beta_R} \]  

(9.16)

where

\( \beta_F \) is the transistor current gain caused by emitter injection efficiency
\( \beta_T \) is the transistor current gain caused by base transport efficiency
\( \beta_R \) is the recombination component of the current gain

As one can see from Equation 9.16, smaller values of \( \beta_F \), \( \beta_T \), and \( \beta_R \) dominate. The base transport efficiency can be defined as a ratio of injected carriers into the base, to the carriers that recombine within the base.
This ratio is also equal to the ratio of the minority carrier’s lifetime to the transit time of carriers through the base. The carrier transit time can be approximated by an empirical relationship

\[
\tau_{\text{transit}} = \frac{w_B}{V_T \mu_B (2 + 0.9 \eta)}; \quad \eta = \ln \left( \frac{N_{\text{RE}}}{N_{\text{BC}}} \right)
\]

(9.17)

where
- \(\mu_B\) is the mobility of the minority carriers in base
- \(w_B\) is the base thickness
- \(N_{\text{RE}}\) is the impurity doping level at the emitter side of the base
- \(N_{\text{BC}}\) is the impurity doping level at the collector side of the base

Therefore, the current gain due to the transport efficiency is

\[
\beta_T = \frac{\tau_{\text{life}}}{\tau_{\text{transit}}} = (2 + 0.9 \eta) \left( \frac{L_B}{w_B} \right)^2
\]

(9.18)

where \(L_B = \sqrt{V_T \mu_B \tau_{\text{life}}}\) is the diffusion length of minority carriers in the base.

The current gain \(\beta_E\), due to the emitter injection efficiency, is given by

\[
\beta_E = \frac{\int_0^{w_E} N_{\text{Eeff}}(x) dx}{\int_0^{w_B} N_B(x) dx}
\]

(9.19)

where
- \(\mu_B\) and \(\mu_E\) are minority carrier mobilities in the base and in the emitter
- \(N_B(x)\) is the impurity distribution in the base
- \(N_{\text{Eeff}}\) is the effective impurity distribution in the emitter

The recombination component of the current gain \(\beta_R\) is caused by the different current–voltage relationship of base and collector currents as can be seen in Figure 9.2. The slower base current increase is due to the recombination phenomenon within the depletion layer of the base-emitter junction. Since the current gain is a ratio of the collector current to that of the base current the relation for \(\beta_R\) can be found as

\[
\beta_R = K_{\text{RE}} \frac{1}{e^{\left(1/\eta K\right)}}
\]

(9.20)

As can be seen from Figure 9.2, the current gain \(\beta\) is a function of the current. The gain–current relationship is illustrated in Figure 9.3. The range of a constant current gain is wide for bipolar transistors with a technology characterized by a lower number of generation–recombination centers.

With an increase of the collector–base voltage, the depletion layer penetrates deeper into the base. Therefore, the effective thickness of the base decreases. This leads to an increase of transistor current gain with applied collector voltages. Figure 9.4 illustrates this phenomenon known as Early’s effect. The extensions of transistor characteristics (dotted lines in Figure 9.4) are crossing the voltage axis at the point—\(V_A\), where \(V_A\) is known as the Early voltage. The current gain \(\beta\), as a function of the collector voltage, is usually expressed by using the relation
A similar equation can be defined for the reverse mode of operation.

### 9.4 High Current Phenomena

The concentration of minority carriers increases with the rise of transistor currents. When the concentration of moving carriers exceeds a certain limit, the transistor property degenerates. Two phenomena are responsible for this limitation. The first is related to the high concentration of moving carriers (electrons in the n-p-n transistor) in the base-collector depletion region. This is known as the Kirk effect. The second phenomenon is caused by a high level of carriers injected into the base. When the concentration of injected minority carriers in the base exceeds the impurity concentration there, then the base conductivity modulation limits the transistor’s performance.

To understand the Kirk effect, consider the NPN transistor in the forward-active mode with the base-collector junction reversely biased. The depletion layer consists of the negative lattice charge of the base region and the positive lattice charge of the collector region. Boundaries of the depletion layer are such that the total positive and negative charges are equal. When a collector current that carries the negatively charged electrons flows through the junction, the effective negative charge on the base side of the junction increases. Also, the positive lattice charge of the collector side of the junction is compensated by the negative charge of moving electrons. As a result, the collector-base space charge region moves toward the collector, resulting in a thicker effective base. With a large current level, the thickness of the

\[
\beta = \beta_0 \left(1 + \frac{V_{CE}}{V_A}\right)
\]  

(9.21)
base may be doubled or tripled. This phenomenon, known as the Kirk effect, becomes very significant when the charge of moving electrons exceeds the charge of the lightly doped collector $N_C$. The threshold current for the Kirk effect is given by

$$I_{\text{max}} = qA\nu_{\text{sat}}N_C$$

(9.22)

where $\nu_{\text{sat}}$ is the saturation velocity for electrons ($\nu_{\text{sat}} = 10^7$ cm/s for silicon).

The conductivity modulation in the base, or high-level injection, starts when the concentration of injected electrons into the base exceeds the lowest impurity concentration in the base $N_{B\text{min}}$. This occurs for the collector current $I_{\text{max}}$ given by

$$I_{\text{max}} < qA\nu_{\text{sat}}N_C < qA\nu_{\text{sat}}N_C = qAVT\mu_A N_{B\text{max}} (2 + 0.9\eta)$$

(9.23)

The above equation is derived using (9.17), for the estimation of the base transient time.

The high current phenomena are significantly enlarged by the current crowding effect. The typical cross section of the bipolar transistor is shown in Figure 9.5. The horizontal flow of the base current results in the voltage drop across the base region under the emitter. This small voltage difference on the base–emitter junction causes a significant difference in the current densities at the junction. This is due to the very nonlinear junction–current–voltage characteristics. As a result, the base–emitter junction has very nonuniform current distribution across the junction. Most of the current flows through the part of the junction closest to base contact. For transistors with larger emitter areas, the current crowding effect is more significant. This nonuniform transistor current distribution makes the high current phenomena, such as the base conductivity modulation and the Kirk effect, start for smaller currents than given by Equations 9.22 and 9.23. The current crowding effect is also responsible for the change of the effective base resistance with a current. As a base current increases, the larger part of the emitter current flows closer to the base contact, and the effective base resistance decreases.

### 9.5 Small Signal Model

Small signal transistor models are essential for the design of an AC circuit. The small signal equivalent circuit of the bipolar transistor is shown in Figure 9.6a. The lumped circuit shown in Figure 9.6a is only an approximation. In real transistors, resistances and capacitances have a distributed character. For most design tasks, this lumped model is adequate, or even the simple equivalent transistor model shown in Figure 9.6b can be considered. The small signal resistances, $r_x$ and $r_y$, are inversely proportional to the transistor currents, and the transconductance $g_m$ is directly proportional to the transistor currents.
Bipolar Junction Transistor

\[ r_x = \frac{\eta_F V_T}{I_B} = \frac{\eta_F V_T \beta_F}{I_C}; \quad r_0 = \frac{V_A}{I_C}; \quad g_m = \frac{I_C}{\eta_F V_T} \] (9.24)

where
- \( \eta_F \) is the forward emission coefficient, ranging from 1.0 to 2.0
- \( V_T \) is the thermal potential (\( V_T = 25 \text{ mV at room temperature} \))

Similar equations to (9.24) can be written for the reverse transistor operation as well.

\[ r_x = \frac{\eta_F V_T}{I_B} = \frac{\eta_F V_T \beta_F}{I_C}; \quad r_0 = \frac{V_A}{I_C}; \quad g_m = \frac{I_C}{\eta_F V_T} \] (9.25)

where
- \( I_{KF} \) is \( \beta_F \) high-current roll-off current
- \( R_{B0} \) is the base resistance at very small currents
- \( R_{B_{min}} \) is the minimum base resistance at high currents

Another possible approximation of the base series resistance \( R_B \) as the function of the base current \( I_B \), is [4]

\[ R_B = 3 \left( R_{B0} - R_{B_{min}} \right) \tan z - z + R_{B_{min}} \quad z = \frac{1 + (1.44 I_B \pi^2 I_{RB}) - 1}{(24\pi^2)\sqrt{(I_B/I_{RB})}} \] (9.26)

where \( I_{RB} \) is the base current for which the base resistance falls halfway to its minimum value.
The base–emitter capacitance $C_{BE}$ is composed of two terms: the diffusion capacitance, which is proportional to the collector current, and the depletion capacitance, which is a function of the base–emitter voltage $V_{BE}$. The $C_{BE}$ capacitance is given by

$$C_{BE} = \tau_F \frac{I_C}{\eta_F V_T} + C_{JEO} \left(1 - \frac{V_{BE}}{V_{JEO}}\right)^{-m_{JE}}$$  \hspace{1cm} (9.27)$$

where

- $V_{JEO}$ is the base–emitter junction potential
- $\tau_F$ is the base transit time for the forward direction
- $C_{JEO}$ is base–emitter zero-bias junction capacitance
- $m_{JE}$ is the base–emitter grading coefficient

The base–collector capacitance $C_{BC}$ is given by a similar expression as Equation 9.27. In the case when the transistor operates in the forward-active mode, it can be simplified to

$$C_{BC} = C_{JCO} \left(1 - \frac{V_{BC}}{V_{JCO}}\right)^{-m_{JC}}$$  \hspace{1cm} (9.28)$$

where

- $V_{JCO}$ is the base–collector junction potential
- $C_{JCO}$ is the base–collector zero-bias junction capacitance
- $m_{JC}$ is the base–collector grading coefficient

In the case when the bipolar transistor is in the integrated form, the collector–substrate capacitance $C_{CS}$ has to be considered

$$C_{CS} = C_{JSO} \left(1 - \frac{V_{CS}}{V_{JSO}}\right)^{-m_{JS}}$$  \hspace{1cm} (9.29)$$

where

- $V_{JSO}$ is the collector–substrate junction potential
- $C_{JSO}$ is the collector–substrate zero-bias junction capacitance
- $m_{JS}$ is the collector–substrate grading coefficient

When the transistor enters saturation, or it operates in the reverse-active mode, Equations 9.27 and 9.28 should be modified to

$$C_{BE} = \tau_S \frac{I_S \exp\left(\frac{V_{BE}}{\eta_F V_T}\right)}{\eta_F V_T} + C_{JEO} \left(1 - \frac{V_{BE}}{V_{JEO}}\right)^{-m_{JE}}$$  \hspace{1cm} (9.30)$$

$$C_{BC} = \tau_R \frac{I_S \exp\left(\frac{V_{BC}}{\eta_R V_T}\right)}{\eta_R V_T} + C_{JCO} \left(1 - \frac{V_{BC}}{V_{JCO}}\right)^{-m_{JC}}$$  \hspace{1cm} (9.31)$$

9.6 Technologies

The bipolar technology was used to fabricate the first integrated circuits more than 40 years ago. A similar standard bipolar process is still used. In recent years, for high performance circuits and for BiCMOS technology, the standard bipolar process was modified by using the thick selective silicon oxidation instead of
the p-type isolation diffusion. Also, the diffusion process was substituted by the ion implantation process, low temperature epitaxy, and CVD.

### 9.6.1 Integrated NPN Bipolar Transistor

The structure of the typical integrated bipolar transistor is shown in Figure 9.7. The typical impurity profile of the bipolar transistor is shown in Figure 9.8. The emitter doping level is much higher than the base doping, so large current gains are possible (see Equation 9.19). The base is narrow and it has an impurity gradient, so the carrier transit time through the base is short (see Equation 9.17). Collector concentration near the base collector junction is low, therefore, the transistor has a large breakdown voltage, large Early voltage $V_{AF}$, and collector–base depletion capacitance is low. High impurity concentration in the buried layer leads to a small collector series resistance. The emitter strips have to be as narrow as technology allows, reducing the base series resistance and the current crowding effect. If large emitter area is required, many narrow emitter strips interlaced with base contacts have to be used in a single transistor. Special attention has to be taken during the circuit design, so the base–collector junction is not forward biased. If the base–collector junction is forward biased, then the parasitic PNP transistors activate. This leads to an undesired circuit operation. Thus, the integrated bipolar transistors must not operate in reverse or in saturation modes.

![FIGURE 9.7 NPN bipolar structure.](image)

![FIGURE 9.8 Cross section of a typical bipolar transistor.](image)
9.6.2 Lateral and Vertical PNP Transistors

The standard bipolar technology is oriented for the fabrication of the NPN transistors with the structure shown in Figure 9.7. Using the same process, other circuit elements, such as resistors and PNP transistors, can be fabricated as well.

A lateral transistor, shown in Figure 9.9a, uses the base p-type layer for both the emitter and collector fabrications. A vertical transistor, shown in Figure 9.9b, uses the p-type base layer for the emitter, and the p-type substrate as the collector. This transistor is sometimes known as the substrate transistor. In both transistors, the base is made of the n-type epitaxial layer. Such transistors with a uniform and thick base are slow. Also, the current gain \( \beta \) of such transistors is small. Note, that the vertical transistor has the collector shorted to the substrate as Figure 9.10b illustrates. When a PNP transistor with a large current gain is required, then the concept of the composite transistor can be implemented. Such a composite transistor, known also as the super-beta transistor, consists of a PNP lateral transistor, and the standard NPN transistor is connected, as shown in Figure 9.10c. A composed transistor acts as the PNP transistor and it has a current gain \( \beta \) approximately equal to \( \beta_{pnp} \beta_{npn} \).

9.7 Model Parameters

It is essential to use proper transistor models in the computer aided design tools. The accuracy of simulation results depends on the model's accuracy, and on the values of the model parameters used. In this subchapter, the thermal and second order effects in the transistor model are discussed. The SPICE bipolar transistor model parameters are also discussed.
9.7.1 Thermal Sensitivity

All parameters of the transistor model are temperature dependent. Some parameters are very strong functions of temperature. To simplify the model description, the temperature dependence of some parameters is often neglected. In this chapter, the temperature dependence of the transistor model is described based on the model of the SPICE program [3–5]. Deviations from the actual temperature dependence will also be discussed. The temperature dependence of the junction capacitance is given by

\[
C_J(T) = C_J \left[ 1 + m_1 \left( 4.0 \times 10^{-4} (T - T_{\text{NOM}}) + \left( V_J(T) - \frac{V_J(T)}{V_J} \right) \right) \right]
\]

where \( T_{\text{NOM}} \) is the nominal temperature, which is specified in the SPICE program in the .OPTIONS statement. The junction potential \( V_J(T) \) is a function of temperature

\[
V_J(T) = V_J - 3V_J \ln \left( \frac{T}{T_{\text{NOM}}} \right) - E_G(T) + \frac{E_G}{T_{\text{NOM}}}
\]

The transistor saturation current as a function of temperature is calculated as

\[
I_s(T) = I_s \left( \frac{T}{T_{\text{NOM}}} \right)^{X_{\text{TH}}} \exp \left[ \frac{E_G(T - T_{\text{NOM}})}{V_J T_{\text{NOM}}} \right]
\]

where \( E_G \) is the energy gap at the nominal temperature. The value of 3, in the multiplication coefficient of above equation is from the temperature dependence of the effective state densities in the valence and conduction bands. The temperature dependence of the energy gap is computed in the SPICE program from

\[
E_G(T) = E_G - \frac{7.02 \times 10^{-4} T^2}{T + 1108}
\]

The temperature dependence of the transistor current gains \( \beta_F \) and \( \beta_R \) are modeled in the SPICE as

\[
\beta_F(T) = \beta_F \left( \frac{T}{T_{\text{NOM}}} \right)^{X_{\text{TH}}}, \quad \beta_R(T) = \beta_R \left( \frac{T}{T_{\text{NOM}}} \right)^{X_{\text{TH}}}
\]
The SPICE model does not give accurate results for the temperature relationship of the current gain $\beta$ at high currents. For high current levels the current gain decreases sharply with the temperature, as can be seen from Figure 9.3. Also, the knee current parameters $IKF$, $IKR$, $IKB$ are temperature dependent, and this is not implemented in the SPICE program.

### 9.7.2 Second Order Effects

The current gain $\beta$ is sometimes modeled indirectly by using different equations for the collector and base currents [4,5]

$$I_C = \frac{I_s(T)}{Q_b} \left( \exp \frac{V_{BE}}{\eta_b V_T} - \exp \frac{V_{BC}}{\eta_b V_T} \right) - \frac{I_s(T)}{\beta_p(T)} \left( \exp \frac{V_{BC}}{\eta_b V_T} - 1 \right) - I_{SC}(T) \left( \exp \frac{V_{BC}}{\eta_c V_T} - 1 \right)$$

(9.39)

where

$$Q_b = \frac{1 + \sqrt{1 + 4Q_N}}{2(1 - (V_{BC}/V_{AF}) - (V_{BE}/V_{AS}))}$$

(9.40)

and

$$Q_x = \frac{I_s(T)}{I_{KF}} \left( \exp \frac{V_{BE}}{\eta_b V_T} - 1 \right) + \frac{I_s(T)}{I_{KR}} \left( \exp \frac{V_{BC}}{\eta_b V_T} - 1 \right)$$

(9.41)

$$I_B = \frac{I_s}{\beta_p} \left( \exp \frac{V_{BE}}{\eta_b V_T} - 1 \right) + I_{SE} \left( \exp \frac{V_{BE}}{\eta_e V_T} - 1 \right) + \frac{I_s}{\beta_R} \left( \exp \frac{V_{BC}}{\eta_b V_T} - 1 \right) + I_{SC} \left( \exp \frac{V_{BC}}{\eta_c V_T} - 1 \right)$$

(9.42)

where

- $I_{BE}$ is the base–emitter junction leakage current
- $I_{SC}$ is the base–collector junction leakage current
- $\eta_b$ is the base–emitter junction leakage emission coefficient
- $\eta_c$ is the base–collector junction leakage emission coefficient

The forward transit time $\tau_F$ is a function of biasing conditions. In the SPICE program the $\tau_F$ parameter is computed by using

$$\tau_F = \tau_{FB} \left[ 1 + X_{TF} \left( \frac{I_{CC}}{I_{CC} + I_{TF}} \right) \exp \frac{V_{BC}}{1.44 V_{TF}} \right] I_{CC} = I_S \left( \exp \frac{V_{BE}}{\eta_b V_T} - 1 \right)$$

(9.43)

At high frequencies the phase of the collector current shifts. This phase shift is computed in the SPICE program in the following way:

$$I_C(\omega) = I_C \exp \left( j\omega P_{TF} \tau_F \right)$$

(9.44)

where $P_{TF}$ is a coefficient for excess phase calculation.

Noise is usually modeled as the thermal noise for parasitic series resistances, and as shot and flicker noise for collector and base currents

$$I_n = \frac{4kT \Delta f}{R}$$

(9.45)
where $K_F$ and $A_F$ are the flicker noise coefficients. More detailed information about noise modeling

$$\overline{i_F} = \left(2qI_n + \frac{K_FL_n}{F}\right)\Delta f$$ (9.46)

$$\overline{i_c} = 2qI_c\Delta f$$ (9.47)

is given in the bipolar noise chapter of this handbook.

### 9.7.3 SPICE Model of the Bipolar Transistor

The SPICE model of the bipolar transistor uses similar or identical equations as described in this chapter [3–5]. Table 9.1 shows the parameters of the bipolar transistor model and its relation to the parameters used in this chapter.

SPICE (Simulation Program with Integrated Circuit Emphasis [3]) was developed mainly for the analysis of integrated circuits. During the analysis, it is assumed that the temperatures of all circuit elements are the same. This is not true for power integrated circuits where the junction temperatures may differ by 30 K or more. This is obviously not true for circuits composed of the discrete elements where the junction temperatures may differ by 100 K and more. These temperature effects, which can significantly affect the analysis results, are not implemented in the SPICE program.

Although the SPICE bipolar transistor model uses more than 40 parameters, many features of the bipolar transistor are not included in the model. For example, the reverse junction characteristics are described by Equation 9.32. The model does not give accurate results. In the real silicon junction, the leakage current is proportional to the thickness of the depletion layer, which is proportional to $V^{1/6}$. Also, the SPICE model of the bipolar transistor assumes that there is no junction breakdown voltage. A more accurate model of the reverse junction characteristics is described in the diode section of this handbook. The reverse transit time $\tau_R$ is very important to model the switching property of the lumped bipolar transistor, and it is a strong function of the biasing condition and the temperature. Both phenomena are not implemented in the SPICE model.

### 9.8 SiGe HBTs

The performance of the Si bipolar transistor can be greatly enhanced with proper engineering of the base bandgap profile using a narrower bandgap material, SiGe, an alloy of Si and Ge. Structure wise, a SiGe HBT is essentially a Si BJT with a SiGe base. Its operation and circuit level performance advantages can be illustrated with the energy band diagram in Figure 9.11 [13]. Here the Ge content is linearly graded from the emitter toward the collector to create a large accelerating electric field that speeds up the minority carrier transport across the base, thus making the transistor speed much faster and the cutoff frequency much higher. Everything else being the same, the potential barrier for electron injection into the base is reduced, thus exponentially enhancing the collector current. The base current is the same for SiGe HBT and Si BJT, as the emitter is typically made the same. Beta is thus higher in SiGe HBT. Figure 9.12 confirms these expectations experimentally with the data from a typical first generation SiGe HBT technology. The measured doping and Ge profiles are shown in Figure 9.13. The metallurgical base width is only 90 nm, and the neutral base width is around 50 nm. Figure 9.14 shows the experimental cutoff frequency $f_c$ improvement from using a graded SiGe base, which also directly translates into maximum oscillation frequency $f_{max}$ improvement.
## TABLE 9.1 Parameters of SPICE Bipolar Transistor Model

<table>
<thead>
<tr>
<th>Name Used</th>
<th>Equations</th>
<th>SPICE Name</th>
<th>Parameter Description</th>
<th>Unit</th>
<th>Typical Value</th>
<th>SPICE Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_s$</td>
<td>10, 11</td>
<td>IS</td>
<td>Saturation current</td>
<td>A</td>
<td>$10^{-15}$</td>
<td>$10^{-16}$</td>
</tr>
<tr>
<td>$I_{SE}$</td>
<td>39</td>
<td>ISE</td>
<td>B–E leakage saturation current</td>
<td>A</td>
<td>$10^{-12}$</td>
<td>0</td>
</tr>
<tr>
<td>$I_{SC}$</td>
<td>39</td>
<td>ICS</td>
<td>B–C leakage saturation current</td>
<td>A</td>
<td>$10^{-12}$</td>
<td>0</td>
</tr>
<tr>
<td>$\beta_F$</td>
<td>14, 16, 21</td>
<td>BF</td>
<td>Forward current gain</td>
<td>—</td>
<td>100</td>
<td>100</td>
</tr>
<tr>
<td>$\beta_R$</td>
<td>14, 16, 21</td>
<td>BF</td>
<td>Reverse current gain</td>
<td>—</td>
<td>0.1</td>
<td>1</td>
</tr>
<tr>
<td>$\eta_F$</td>
<td>15, 24, 30, 31, 39–41</td>
<td>NF</td>
<td>Forward current emission coefficient</td>
<td>—</td>
<td>1.2</td>
<td>1.0</td>
</tr>
<tr>
<td>$\eta_R$</td>
<td>15, 24, 30, 31, 39–42</td>
<td>NR</td>
<td>Reverse current emission coefficient</td>
<td>—</td>
<td>1.3</td>
<td>1.0</td>
</tr>
<tr>
<td>$\eta_E$</td>
<td>39</td>
<td>NE</td>
<td>B–E leakage emission coefficient</td>
<td>—</td>
<td>1.4</td>
<td>1.5</td>
</tr>
<tr>
<td>$\eta_C$</td>
<td>39</td>
<td>NC</td>
<td>B–C leakage emission coefficient</td>
<td>—</td>
<td>1.4</td>
<td>1.5</td>
</tr>
<tr>
<td>$V_{AF}$</td>
<td>21, 40</td>
<td>VAF</td>
<td>Forward Early voltage</td>
<td>V</td>
<td>200</td>
<td>∞</td>
</tr>
<tr>
<td>$V_{AR}$</td>
<td>21, 40</td>
<td>VAR</td>
<td>Reverse Early voltage</td>
<td>V</td>
<td>50</td>
<td>∞</td>
</tr>
<tr>
<td>$I_{KF}$</td>
<td>22, 23, 40</td>
<td>IKF</td>
<td>$\beta_h$ high current roll-off corner</td>
<td>A</td>
<td>0.05</td>
<td>∞</td>
</tr>
<tr>
<td>$I_{KR}$</td>
<td>22, 23, 40</td>
<td>IKR</td>
<td>$\beta_h$ high current roll-off corner</td>
<td>A</td>
<td>0.01</td>
<td>∞</td>
</tr>
<tr>
<td>$I_{RB}$</td>
<td>26</td>
<td>IRB</td>
<td>Current where base resistance falls by half</td>
<td>A</td>
<td>0.1</td>
<td>∞</td>
</tr>
<tr>
<td>$R_B$</td>
<td>25, 26</td>
<td>RB</td>
<td>Zero base resistance</td>
<td>Ω</td>
<td>100</td>
<td>0</td>
</tr>
<tr>
<td>$R_{Bmin}$</td>
<td>25, 26</td>
<td>RBM</td>
<td>Minimum base resistance</td>
<td>Ω</td>
<td>10</td>
<td>RB</td>
</tr>
<tr>
<td>$R_E$</td>
<td>Figure 9.6</td>
<td>RE</td>
<td>Emitter series resistance</td>
<td>Ω</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>$R_C$</td>
<td>Figure 9.6</td>
<td>RC</td>
<td>Collector series resistance</td>
<td>Ω</td>
<td>50</td>
<td>0</td>
</tr>
<tr>
<td>$C_{JE0}$</td>
<td>27</td>
<td>CJJE</td>
<td>B–E zero-bias depletion capacitance</td>
<td>F</td>
<td>$10^{-12}$</td>
<td>0</td>
</tr>
<tr>
<td>$C_{JC0}$</td>
<td>28</td>
<td>CJJC</td>
<td>B–C zero-bias depletion capacitance</td>
<td>F</td>
<td>$10^{-12}$</td>
<td>0</td>
</tr>
<tr>
<td>$C_{JS0}$</td>
<td>29</td>
<td>CJS</td>
<td>Zero-bias collector–substrate capacitance</td>
<td>F</td>
<td>$10^{-12}$</td>
<td>0</td>
</tr>
<tr>
<td>$V_{JE0}$</td>
<td>27</td>
<td>VJE</td>
<td>B–E built-in potential</td>
<td>V</td>
<td>0.8</td>
<td>0.75</td>
</tr>
<tr>
<td>$V_{JCB}$</td>
<td>28</td>
<td>VJC</td>
<td>B–C built-in potential</td>
<td>V</td>
<td>0.7</td>
<td>0.75</td>
</tr>
<tr>
<td>$V_{JSD}$</td>
<td>29</td>
<td>VJS</td>
<td>Substrate junction built-in potential</td>
<td>V</td>
<td>0.7</td>
<td>0.75</td>
</tr>
<tr>
<td>$m_{JE}$</td>
<td>27</td>
<td>MJE</td>
<td>B–E junction exponential factor</td>
<td>—</td>
<td>0.33</td>
<td>0.33</td>
</tr>
<tr>
<td>$m_{JC}$</td>
<td>28</td>
<td>MJC</td>
<td>B–C junction exponential factor</td>
<td>—</td>
<td>0.5</td>
<td>0.33</td>
</tr>
<tr>
<td>$m_{JS}$</td>
<td>29</td>
<td>MJS</td>
<td>Substrate junction exponential factor</td>
<td>—</td>
<td>0.5</td>
<td>0</td>
</tr>
<tr>
<td>$X_{CJC}$</td>
<td>Figure 9.6</td>
<td>XCJC</td>
<td>Fraction of B–C capacitance connected to internal base node (see Figure 9.6)</td>
<td>—</td>
<td>0.5</td>
<td>0</td>
</tr>
<tr>
<td>$\tau_F$</td>
<td>17, 28, 30, 42</td>
<td>TF</td>
<td>Ideal forward transit time</td>
<td>s</td>
<td>$10^{-10}$</td>
<td>0</td>
</tr>
<tr>
<td>$\tau_R$</td>
<td>31</td>
<td>TR</td>
<td>Reverse transit time</td>
<td>s</td>
<td>$10^{-8}$</td>
<td>0</td>
</tr>
<tr>
<td>$X_{TP}$</td>
<td>43</td>
<td>XTF</td>
<td>Coefficient for bias dependence of $\tau_F$</td>
<td>—</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>$V_{TF}$</td>
<td>43</td>
<td>VTF</td>
<td>Voltage for $\tau_F$ dependence on $V_{BC}$</td>
<td>V</td>
<td>∞</td>
<td></td>
</tr>
<tr>
<td>$I_{TF}$</td>
<td>43</td>
<td>ITF</td>
<td>Current where $\tau_F = f(I_C, V_{BC})$ starts</td>
<td>A</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>$P_{TF}$</td>
<td>44</td>
<td>PTF</td>
<td>Excess phase at freq = $1/(2\pi \tau_F)$ Hz</td>
<td>deg</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>$X_{TB}$</td>
<td>38</td>
<td>XTB</td>
<td>Forward and reverse beta temperature exponent</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>$E_G$</td>
<td>34</td>
<td>EG</td>
<td>Energy gap</td>
<td>eV</td>
<td>1.1</td>
<td>1.11</td>
</tr>
<tr>
<td>$X_{TI}$</td>
<td>35–37</td>
<td>XTI</td>
<td>Temperature exponent for effect on $I_s$</td>
<td>—</td>
<td>3.5</td>
<td>3</td>
</tr>
<tr>
<td>$K_F$</td>
<td>46</td>
<td>KF</td>
<td>Flicker-noise coefficient</td>
<td>—</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>$A_F$</td>
<td>46</td>
<td>AF</td>
<td>Flicker-noise exponent</td>
<td>—</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>$F_C$</td>
<td></td>
<td>FC</td>
<td>Coefficient for the forward biased depletion capacitance formula</td>
<td>—</td>
<td>0.5</td>
<td>0.5</td>
</tr>
<tr>
<td>$T_{NOM}$</td>
<td>32–38</td>
<td>TNOM</td>
<td>Nominal temperature specified in OPTION statement</td>
<td>K</td>
<td>300</td>
<td>300</td>
</tr>
</tbody>
</table>
9.8.1 Operation Principle and Performance Advantages over Si BJT

In modern transistors, particularly with the use of polysilicon emitter, beta may be sufficient. If so, the higher beta potential of SiGe HBT can then be traded for reduced base resistance, using higher base doping. The unique ability of simultaneously achieving high beta, low base resistance, and high cutoff frequency makes SiGe HBT attractive for many radio-frequency (RF) circuits. Broadband noise is naturally reduced, as low base resistance reduces transistor input noise voltage, and high beta as well as high $f_T$ reduces transistor input noise current [13]. Experimentally, $1/f$ noise at the same base current was found to be approximately the same for SiGe HBT and Si BJT [14]. Consequently, $1/f$ noise is often naturally reduced in SiGe HBT circuits for the same biasing collector current, as the base current is often smaller due to a higher beta, as shown in Figure 9.15, by using the corner frequency as a figure-of-merit.
These, together with circuit level optimization can lead to excellent low phase noise oscillators and frequency synthesizers suitable for both wireless and wire line communication circuits. Another less obvious advantage from grading Ge is the collector side of the neutral base that has less impact on the collector current than the emitter side of the neutral base. Consequently, as the collector voltage varies and the collector side of the neutral base is shifted toward the emitter due to increased CB junction-depletion layer thickness, the collector current is increased to a much lesser extent than in a comparably constructed Si BJT, leading to a much higher output impedance or Early voltage. The $β × V_A$ product is thus much higher in SiGe HBT than in Si BJT.

### 9.8.2 Industry Practice and Fabrication Technology

The standard industry practice today is to integrate SiGe HBT with CMOS to form a SiGe BiCMOS technology. The ability to integrate with CMOS is also a significant advantage of SiGe HBT over III–V HBT. Modern SiGe BiCMOS combines the analog and RF performance advantages of the SiGe HBT,
and the lower power logic, high integration level, and memory density of Si CMOS, into a single cost effective system-on-chip (SoC) solution. Typically, SiGe HBTs with multiple breakdown voltages are offered through the selective collector implantation, to provide more flexibility in the circuit design.

The fabrication process of SiGe HBT and its integration with CMOS has been constantly evolving in the past two decades, and varies from company to company. Below are some common fabrication elements and modules shared by many, if not all, commercial first generation (also most widespread in manufacturing at present) SiGe technologies:

1. A starting N⁺ subcollector around 5 Ω/square on a p-type substrate at 5 × 10¹⁵/cm³, typically patterned to allow CMOS integration.
2. A high temperature, lightly doped n-type collector, around 0.4–0.6 μm thick at 5 × 10¹⁵/cm³.
3. Polysilicon filled deep trenches for isolation from adjacent devices, typically 1 μm wide and 7–10 μm deep.
4. Oxide filled shallow trenches or LOCOS for local device isolation, typically 0.3–0.6 μm deep.

FIGURE 9.15  Experimentally measured corner frequency as a function of collector current density for three SiGe HBTs with different base SiGe designs, and a comparatively constructed Si BJT.

FIGURE 9.16  Structure of a modern SiGe HBT.
5. An implanted collector reaches through to the subcollector, typically at 10–20 Ωμm².
6. A composite SiGe epilayer consisting of a 10–20 nm Si buffer, a 70–100 nm boron-doped SiGe active layer, with or without C doping to help suppress boron out diffusion, and a 10–30 nm Si cap. The integrated boron dose is typically 1–3 × 10¹³/cm².
7. A variety of emitter–base self-alignment scheme, depending on the device structure and SiGe growth approach. All of them utilize some sort of spacer that is 100–300 nm wide.
8. Multiple self-aligned collector implantations to allow multiple breakdown voltages on the same chip.
9. Polysilicon extrinsic base, usually formed during SiGe growth over shallow trench oxide, and additional self-aligned extrinsic implantation to lower base resistance.
10. A silicided extrinsic base.
11. A 100–200 nm thick heavily doped (>5 x 10²⁰/cm³) polysilicon emitter, either implanted or in situ doped.
12. A variety of multiple level back-end-of-line metallization schemes using Al or Cu, typically borrowed from the parent CMOS process.

These technological elements can also be seen in the electronic image of a second generation SiGe HBT shown in Figure 9.16.

References
