The number of devices of SID family is growing with time. The static induction transistors can operate with power of 100kW at 100kHz or 10W at 10GHz. Static induction transistor logic had 100 time smaller switching energy than its I/L competitor. Static induction thyristor has many advantages over the traditional SCR, and Static induction diode exhibits high switching speed, large reverse voltage and low forward voltage drops. There are many devices which belong to the static induction devices family: Static Induction Transistor (SIT), Static Induction Diode (SID), Static Induction Thyristor, Static Induction MOS Transistor (SIMOS), and Space Charge Limiting Load (SCLL) the examples.

Theory of Static Induction Devices (3)

Samples of the potential distribution in SIT devices are shown below. The vicinity of the potential barrier was approximated using parabolic formulas along and across the channel.

Potential distribution in SIT (a) view from the source side and (b) view from the drain side.

Theory of Static Induction Devices (4)

Potential distribution in the vicinity of the barrier approximated by parabolic shapes.

\[ J_s = \frac{qD_s N_x}{V_T} \left[ \int \exp \left( \frac{-\phi(x)}{V_T} \right) dx \right] \]

where \( \phi(x) \) is the potential barrier height in reference to the source potential, \( N_x \) is the electron concentration at the source, \( W/L \) ratio describes the shape of the potential saddle in vicinity of the barrier, and \( Z \) is the length of the source strip.

Cross section of the Static Induction Transistor and typical characteristics [Nishizawa75]
Theory of Static Induction Devices (5)

Since barrier height $\Phi$ can be a linear function of gate and drain voltages, therefore

$$I_g = qD_n N_p W \exp\left(\frac{-\Phi}{kT}\right)$$

$$I_g = qD_n N_p W \exp\left(\frac{-\sigma(V_{gds} + V_{ds} + \Phi_s)}{kT}\right)$$

For large current levels the device current is controlled by the space charge of moving carriers. In the one-dimensional case the potential distribution is described by the Poisson equation:

$$\frac{d^2\phi}{dx^2} = -\frac{\rho(x)}{\varepsilon \varepsilon_0} = \frac{I_{DS}}{A V(x)}$$

For a small electrical fields $\psi(x)=\mu E(x)$

$$I_{DS} = \frac{9}{8} \frac{V_{DS}^2 \mu \varepsilon \varepsilon_0 A}{L^2}$$

For a large electrical field $\psi(x) = \text{const}$

$$I_{DS} = 2 \frac{V_{DS} \mu \varepsilon \varepsilon_0 A}{L^2}$$

Static Induction Transistor (SIT)

(transient response)

With diffusion based transport of carriers in the vicinity of the potential barrier the carrier transit time can be estimated using the formula:

$$I_{trans} = I_{eff}^2$$

$$= \frac{D}{\mu \varepsilon \varepsilon_0}$$

where $I_{eff}$ is the effective length of the channel and $D = \mu \varepsilon \varepsilon_0$ is the diffusion constant.

Bipolar Mode Operation of SI devices (BSIT)

Several complex theories for the bipolar mode of operation were developed, but actually the simple formula, derived before, works well not only for the typical mode of SIT operation, but also for the bipolar mode of SIT operation. Furthermore, the same formula works very well for classical bipolar transistors.

For example, in the case of $nnp$ bipolar transistors the potential distribution across the base in reference to emitter potential at the reference impurity level $N_e = N_i$ is described by

$$\phi(x) = V_x \ln \left( \frac{N_e(x)}{N_i} \right) \exp \left( \frac{V_{be}}{V_T} \right)$$

$$J_S = \int_{V_T}^{qD_n N_i} \left( \frac{\phi(x)}{V_T} \right) dx$$

$$\Rightarrow \quad J_S = \frac{qD_n N_i^2}{V_T} \int_{V_T}^{N_e(x) dx} \exp \left( \frac{V_{be}}{V_T} \right)$$

If the equation is valid for SIT and BJT then one may assume that it is also valid for the bipolar mode of operation of the SIT transistor.

Bipolar Mode Operation of SI devices (BSIT)

Static Induction Transistor Logic (SITL)

The SITL was proposed by Nishizawa and Wilamowski. This logic circuit has almost 100 times better power-delay product than its PL competitor.
Static Induction Transistor Logic (SITL)

The SI transistor can be also used instead of a Schottky diode to protect a bipolar junction transistor against saturation.

Space Charge Limiting Load (SCLL)

Using the concept of the space-charge limited current flow it is possible to fabricate very large resistors on a very small area.

\[ I_{DS} = 2V_{DS}v_{sat}L \frac{A}{L} \]

The 100kΩ resistor requires only several square µm using 2µm technology.

Lateral Punch-Through Transistor (LPTT)

Fabrications of SI transistors usually require very sophisticated technology. It is much simpler to fabricate a lateral punch-through transistor, which operates on the same principle and has similar characteristics.

Static Induction MOS Transistor (SIMOS)

(a) MOS controlled punch-through transistor (a) transistor in the off state for the negative gate potential and (b) transistor in the on state for the positive gate potential.


Static Induction MOS Transistor (SIMOS)

Such a transistor has several advantages over the traditional MOS transistor.
1. The gate capacitance is very small, since there is no accumulation layer under the gate.
2. Carriers are moving with a velocity close to saturation velocity.
3. Much lower substrate doping and the existing depletion layer lead to smaller drain capacitance.

The device operates in a similar fashion as MOS transistor in subthreshold conditions, but this process occurs at much higher current levels. Such "bipolar mode" of operation may have many advantages in VLSI applications.

Static Induction Thyristor

The current gain of npn transistor should be as large as possible and the current gain of pnp transistor should be small. The product of \( \beta_{npn} \) and \( \beta_{pnp} \) should be larger than one. This can be easily implemented using SI structure.

Silicon Control Rectifier (SCR)

Integrated structure of Silicon Control Rectifier (a) cross-section, (b) equivalent diagram

Silicon Control Rectifier (a) cross-section, (b) equivalent diagram

High performance SCR

Silicon Control Rectifier (a) cross-section, (b) equivalent diagram

Integrated structure of Silicon Control Rectifier (a) cross-section, (b) equivalent diagram

\[ n^+p^n+n^- \] Diode

Let us assume the impurity concentration in \( p \) layer \( N_A = 10^{18} \), thickness of \( n^- \) layer = 100\( \mu \)m, thickness of \( p \) layer 0.01\( \mu \)m. The peak electrical field can be found as

\[ E_{\text{MAX}} = \frac{qN_A}{\epsilon_0} = \frac{1.6 \times 10^{-19} \times 1.01 \times 10^{18} \times 6}{12.83 \times 10^{-14}} = 1.55 \times 10^6 \text{ V/cm} \]

and the forward and reverse voltages are

\[ V_{\text{FORWARD}} = \frac{E_{\text{MAX}} (X_p + X_n)}{2} = 0.15 \text{ V} \]
\[ V_{\text{REVERSE}} = E_{\text{MAX}} X_n = 1500 \text{ V} \]

Another advantage of the \( n^+p^n+n^- \) diode is the very fast switching time because this is basically a device with majority carrier transport.


Conductivity Modulation Transistor

Nonvolatile DRAM

Nonvolatile DRAM