High Speed, High Voltage, and Energy Efficient Static Induction Devices

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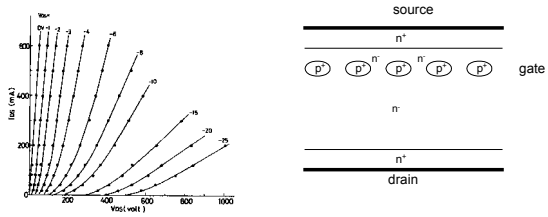
The number of devices of SID family is growing with time. The static induction transistors can operate with power of 100kW at 100kHz or 10W at 10GHz. Static induction transistor logic had 100 time smaller switching energy than its I^2L competitor. Static induction thyristor has many advantages over the traditional SCR, and Static induction diode exhibits high switching speed, large reverse voltage and low forward voltage drops. There are many devices which belong to the static induction devices family: Static Induction Transistor (SIT), Static Induction Diode (SID), Static Induction Thyristor, Lateral Punch-Through Transistor (LPTT), Static Induction Transistor Logic (SITL), Static Induction MOS Transistor (SIMOS), and Space Charge Limiting Load (SCLL) the examples.



Cross section of the Static Induction Transistor and typical characteristics [Nishizawa75]

Theory of Static Induction Devices (1)

For a small electrical field existing in the vicinity of the potential barrier the drift and diffusion current can be approximated by

$$J_n = -qn(x)\mu_n \frac{d\varphi(x)}{dx} + qD_n \frac{dn(x)}{dx}$$

where $D_n = \mu_n V_T$ and $V_T = \frac{kT}{q}$. By multiplying both sides of the equation by $\exp\left(-\frac{\varphi(x)}{V_T}\right)$ and rearranging

$$J_n \exp\left(-\frac{\varphi(x)}{V_T}\right) = qD_n \frac{d}{dx}\left[n(x)\exp\left(-\frac{\varphi(x)}{V_T}\right)\right]$$

Integrating from x_1 to x_2 one can obtain

$$J_n = qD_n \frac{n(x_2)\exp\left(-\frac{\varphi(x_2)}{V_T}\right) - n(x_1)\exp\left(-\frac{\varphi(x_1)}{V_T}\right)}{\int_{x_1}^{x_2} \exp\left(-\frac{\varphi(x)}{V_T}\right)dx}$$

Theory of Static Induction Devices (2)

$$J_n = qD_n \frac{n(x_2)\exp\left(-\frac{\varphi(x_2)}{V_T}\right) - n(x_1)\exp\left(-\frac{\varphi(x_1)}{V_T}\right)}{\int_{x_1}^{x_2} \exp\left(-\frac{\varphi(x)}{V_T}\right)dx}$$

With the following boundary conditions

$$\varphi(x_1) = 0; \quad n(x_1) = N_S;$$
$$\varphi(x_2) = V_D; \quad n(x_2) = N_D;$$

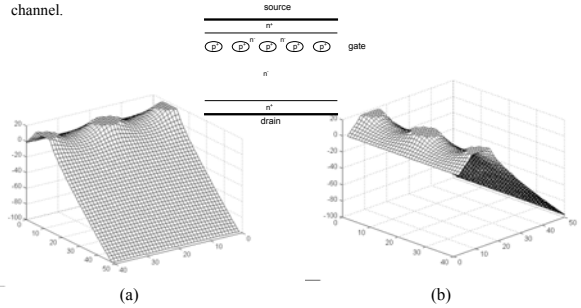
equation (3) reduces to

$$J_n = \frac{qD_n N_S}{\int_{x_1}^{x_2} \exp\left(-\frac{\varphi(x)}{V_T}\right)dx}$$

Note that the above equations derived for SIT can be also used to find current in any devices controlled by a potential barrier, such as a bipolar transistor, MOS transistor operation in subthreshold mode, or in a Schottky diode.

Theory of Static Induction Devices (3)

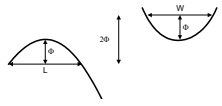
Samples of the potential distribution in SI devices are shown below. The vicinity of the potential barrier were approximated* using parabolic formulas along and across the channel.



(a) (b)

Potential distribution in SIT (a) view from the source side and (b) view from the drain side.

Theory of Static Induction Devices (4)



$$\varphi(y) = \Phi\left[1 - \left(2\frac{y}{W} - 1\right)^2\right]$$
$$\varphi(x) = \Phi\left[1 - \left(2\frac{x}{L} - 1\right)^2\right]$$

Potential distribution in the vicinity of the barrier approximated by parabolic shapes.

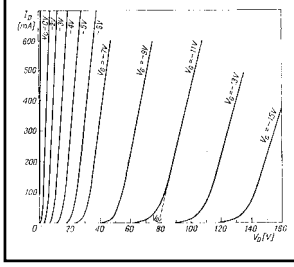
$$J_n = \frac{qD_n N_S}{\int_{x_1}^{x_2} \exp\left(-\frac{\varphi(x)}{V_T}\right)dx} \Rightarrow I_D = qD_p N_S Z \frac{W}{L}\exp\left(\frac{-\Phi}{V_T}\right)$$

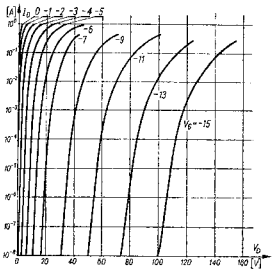
where Φ is the potential barrier height in reference to the source potential, N_S is the electron concentration at the source, W/L ratio describes the shape of the potential saddle in vicinity of the barrier, and Z is the length of the source strip.

Theory of Static Induction Devices (5)

Since barrier height Φ can be a linear function of gate and drain voltages, therefore

$$I_D = qD_p N_S Z \frac{W}{L} \exp\left(\frac{-\Phi}{V_T}\right) \quad \Rightarrow \quad I_D = qD_p N_S Z \frac{W}{L} \exp\left(-\frac{a(V_{GS} + bV_{DS} + \Phi_0)}{V_T}\right)$$





Space charge limited flow

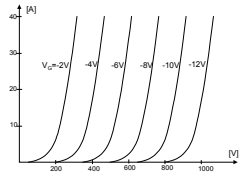
For large current levels the device current is controlled by the space charge of moving carriers. In the one-dimensional case the potential distribution is described by the Poisson equation:

$$\frac{d^2\varphi}{dx_2} = -\frac{\rho(x)}{\varepsilon_{Si}\varepsilon_0} = \frac{I_{DS}}{A\,v(x)}$$

For a small electrical fields $v(x)=\mu E(x)$

$$I_{DS} = \frac{9}{8} V_{DS}^2 \mu \varepsilon_{Si} \varepsilon_0 \frac{A}{L^3}$$

For a large electrical field $v(x)= const$



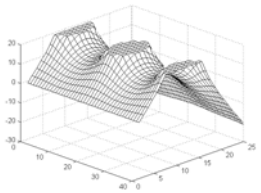
$$I_{DS} = 2V_{DS} v_{sat} \varepsilon_{Si} \varepsilon_0 \frac{A}{L^2}$$

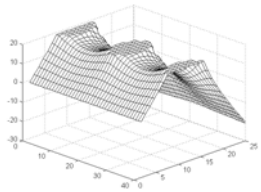
Static Induction Transistor (SIT) (transient response)

With diffusion based transport of carriers in the vicinity of the potential barrier the carrier transit time can be estimated using the formula:

$$t_{trans} = \frac{l_{eff}^2}{D}$$

where l_{eff} is the effective length of the channel and D=μV$_T$ is the diffusion constant





Bipolar Mode Operation of SI devices (BSIT)

Several complex theories for the bipolar mode of operation were developed, but actually the simple formula, derived before, works well not only for the typical mode of SIT operation, but also for the bipolar mode of SIT operation. Furthermore, the same formula works very well for classical bipolar transistors.

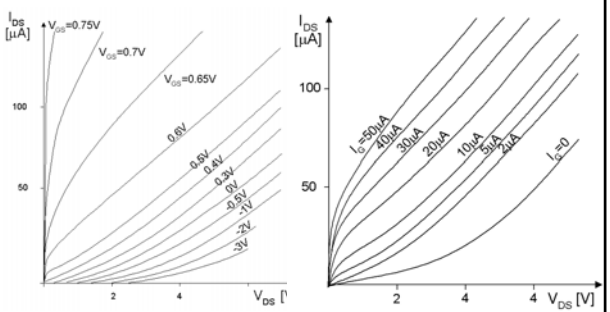
For example, in the case of *npn* bipolar transistors the potential distribution across the base in reference to emitter potential at the reference impurity level $N_E=N_S$ is described by

$$\varphi(x) = V_T \ln\left(\frac{N_B(x)N_S}{n_i^2}\right) \exp\left(-\frac{V_{BE}}{V_T}\right)$$

$$J_n = \frac{qD_n N_S}{\int_{x_1}^{x_2} \exp\left(-\frac{\varphi(x)}{V_T}\right) dx} \quad \Rightarrow \quad J_n = \frac{qD_n n_i^2}{\int_{x_1}^{x_2} N_B(x)dx} \exp\left(\frac{V_{BE}}{V_T}\right)$$

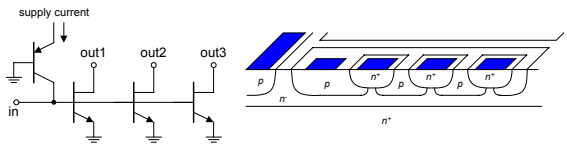
If the equation is valid for SIT and BJT then one may assume that it is also valid for the bipolar mode of operation of the SIT transistor.

Bipolar Mode Operation of SI devices (BSIT)



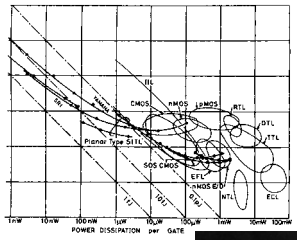
Nishizawa, J. and B. M. Wilamowski, "Static Induction Logic - A Simple Structure with Very Low Switching Energy and Very High Packing Density," *International Conference on Solid State Devices*, Tokyo, Japan, pp. 53-54, 1976 and *Journal of Japanese Soc. Appl. Physics* Vol. **16-1**, pp. 158-162, 1977.

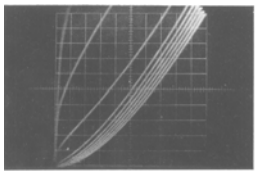
Static Induction Transistor Logic (SITL)

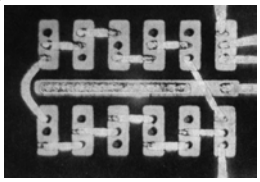


The SITL was proposed by Nishizawa and Wilamowski. This logic circuit has almost 100 times better power-delay product than its I^{2}L competitor.

Static Induction Transistor Logic (SITL)

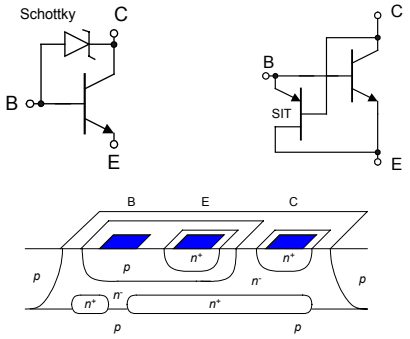






BJT Saturation Protected by SIT

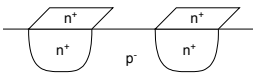
The SI transistor can be also used instead of a Schottky diode to protect a bipolar junction transistor against saturation



Space Charge Limiting Load (SCLL)

Using the concept of the space-charge limited current flow it is possible to fabricate very large resistors on a very small area.

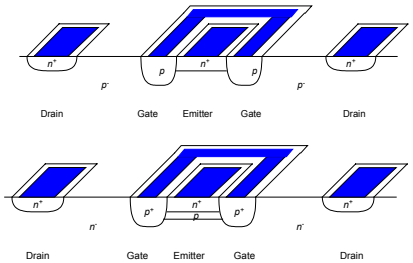
$$I_{DS} = 2V_{DS} v_{sat} \varepsilon_{Si} \varepsilon_0 \frac{A}{L^2}$$



The 100kΩ resistor requires only several square μm using 2μm technology

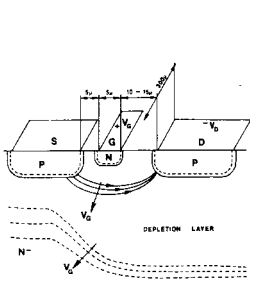
Lateral Punch-Through Transistor (LPTT)

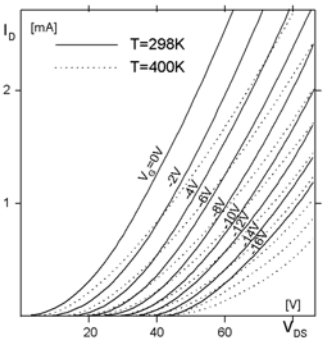
Fabrications of SI transistors usually require very sophisticated technology. It is much simpler to fabricate a lateral punch through transistor, which operates on the same principle and has similar characteristics



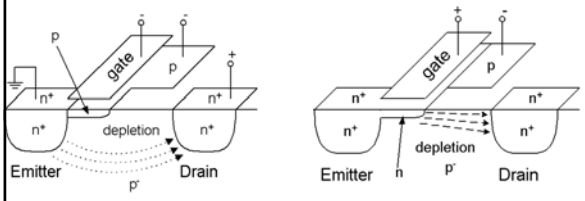
Wilamowski, B. M. and R. C. Jaeger, "The Lateral Punch-Through Transistor," *IEEE Electron Device Letters*, vol. 3, no. 10, pp. 277-280, 1982.

Lateral Punch-Through Transistor (LPTT)





Static Induction MOS Transistor (SIMOS)



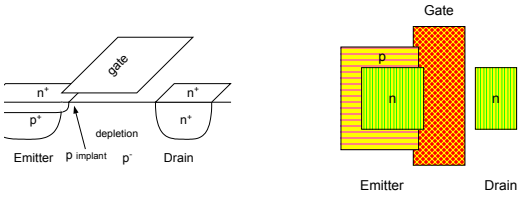
MOS controlled punch-through transistor (a) transistor in the off state for the negative gate potential and (b) transistor in the on state for the positive gate potential.

[1] Wilamowski, B. M., "The Punch-Through Transistor with MOS Controlled Gate," *Phys. Status Solidi (a)*, vol. 79, pp. 631-637, 1983.

[2] Wilamowski, B. M., R. C. Jaeger, and J. N. Fordemwalt, "Buried MOS Transistor with Punch-Through," *Solid State Electronics*, vol. 27, no. 8/9, pp. 811-815, 1984.

Wilamowski, B. M. and R. C. Jaeger, "The Lateral Punch-Through Transistor," *IEEE Electron Device Letters*, vol. 3, no. 10, pp. 277-280, 1982.

Static Induction MOS Transistor (SIMOS)

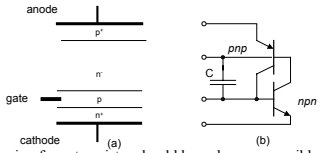


Such a transistor has several advantages over the traditional MOS transistor.

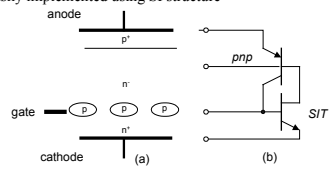
1. The gate capacitance is very small, since there is no accumulation layer under the gate.
2. Carriers are moving with a velocity close to saturation velocity.
3. Much lower substrate doping and the existing depletion layer lead to smaller drain capacitance.

The device operates in a similar fashion as MOS transistor in subthreshold conditions, but this process occurs at much higher current levels. Such "bipolar mode" of operation may have many advantages in VLSI applications.

Static Induction Thyristor

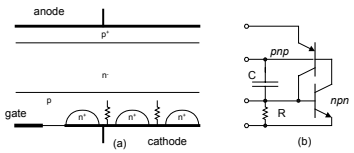


The current gain of *npn* transistor should be as large as possible and the current gain of *pnp* transistor should be small. The product of β_{npn} and β_{pnp} should be larger than one. This can be easily implemented using SI structure

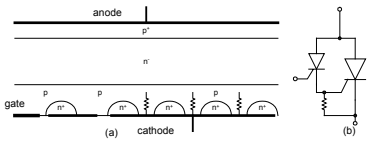


GTO SITh (a) cross-section, (b) equivalent diagram

High performance SCR

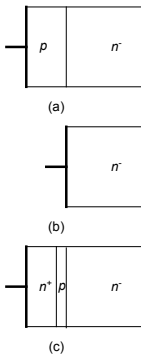


Silicon Control Rectifier (a) cross-section, (b) equivalent diagram



Integrated structure of Silicon Control Rectifier (a) cross-section, (b) equivalent diagram

Punch-Through Emitter



p-n junction

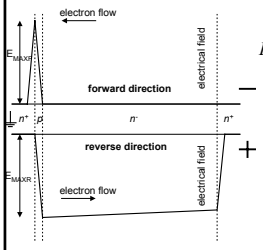
Schottky junction

Punch-through junction

in normal operation condition the p region is depleted from carriers

$n^+pn^-n^+$ Diode

Let us assume the impurity concentration in *p* layer N_A=10^{18}; thickness of n^- layer =100μm, thickness of *p* layer 0.01μm. The peak electrical field can be found as



$$E_{MAX} = \frac{qNx}{\varepsilon_{Si}\varepsilon_0} = \frac{1.6E-19 \cdot 1E18 \cdot 1E-6}{12 \cdot 8.86E-14} = 1.5E5\frac{V}{cm} = 15\frac{V}{\mu m}$$

and the forward and reverse voltages are

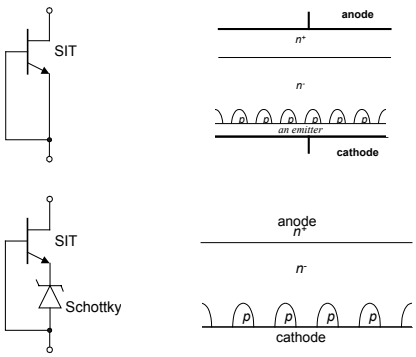
$$V_{FORWARD} \approx \frac{E_{MAX}\left(x_p + x_{n^+}\right)}{2} \approx 0.15\,V$$

$$V_{REVERSE} \approx E_{MAX}\, x_{n^-} = 1500\,V$$

Another advantage of the $n^+pn^-n^+$ diode is the very fast switching time because this is basically a device with majority carrier transport.

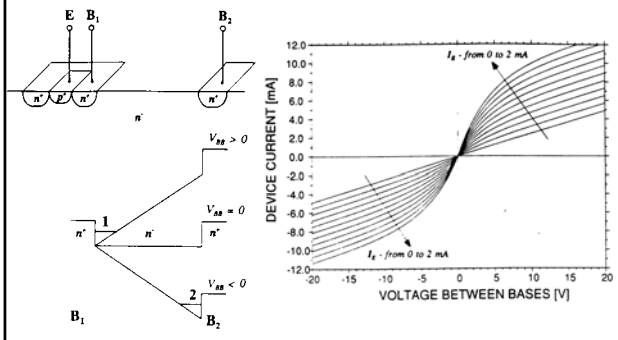
Wilamowski B. M., "High Speed, High Voltage, and Energy Efficient Static Induction Devices" *12 Symposium of Static Induction Devices* - SSID'99, pp. 23-28, April 23, 1999 in Tokyo, Japan

Static Induction Diode (SID)

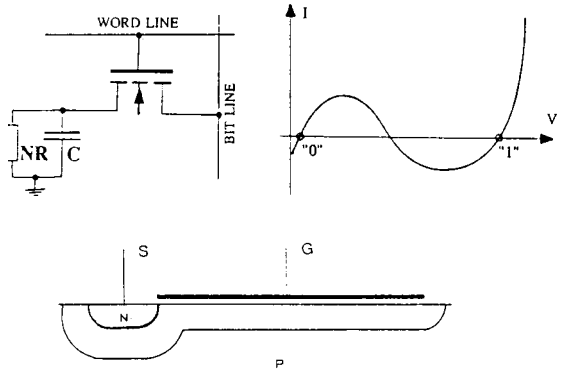


Wilamowski, B. M., "Schottky Diodes with High Breakdown voltage," *Solid-State Electronics*, vol. 26, no. 5, pp. 491-493, 1983.

Conductivity Modulation Transistor



Nonvolatile DRAM



Nonvolatile DRAM