New Graphical I_{DDQ} Signatures Reduce Defect Level and Yield Loss*

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Abstract

The measured I_{DDQ} current as a function of vectors is defined here as the I_{DDQ} signature of a chip. We examined the I_{DDQ} signatures of a large number of SEMATECH chips that have been classified as good or bad by a combined decision from functional, delay and scan tests. We find that a single I_{DDQ} threshold, whether absolute or differential, cannot separate good/bad chips with any desirable accuracy, because the good chip signature can be any one of several well-defined graphs. In general, the signature of a good chip is found to contain discrete levels (or bands) of varying widths and separations. A faulty chip almost always displays noise and glitches in the band structure. Based on observations, we develop a set of five graphical criteria, which provide lower defect level and yield loss compared to other non-I_{DDQ} test methods. The reason is that the graphical procedure customizes the decision for the chip-under-test, and may substantially reduce the usage of other conventional tests.

1 Introduction

I_{DDQ} testing [1] finds defects that are not detectable by voltage tests when the average current caused by a defect is significantly higher than the average quiescent current of good ICs. The variation of quiescent current over a test set, chips, wafers and fabrication processes must be small, and must not affect the classification. This assumption no longer holds for *deep submicron* (DSM) technologies. For DSM devices with high background current, single threshold I_{DDQ} methods result either in unacceptably high levels of *yield loss* (declaring a good chip to be bad), or *test escapes* (declaring a bad chip to be good). Methods were proposed to address the higher leakage current and process and technique variance problems [2, 3, 4, 7, 8, 12], but improved methods are still needed.

This paper introduces a graphical model as a current signature model. Here, the absolute value of I_{DDQ} current measurement is no longer used for the chip pass/fail decision. Instead, the appearance of the measurement over the entire set of test vectors is the factor. This view of I_{DDQ} measurements reflects more physical information for discriminating good and faulty devices than the mean, variance or other comparisons. The self-contained method is not affected by wafer and production process variations. Experiments are done on all SEMATECH data, and the results show significant improvement in yield loss and test escapes. This new discovery may allow I_{DDQ} testing to substantially reduce the usage of other testing methods. Section 2 describes the *devices-under-test* (DUTs). Section 3 describes prior work. Section 4 presents the experiment, analyzes physical phenomena and discusses results. Comparisons appear in Section 5, and Section 6 concludes.

2 Test Chip Description and Classification

SEMATECH data is used in this research. According to Nigh *et al.* [9], five test steps were taken, i.e., wafer level, T0 package level, T1 packaged burn-in level (6 hours), T72 packaged burn-in level (72 hours), and T144 packaged burn-in level (144 hours). In each step, four kinds of tests were applied to each device: Stuck-at tests (8,023 patterns with 99.79% stuck-fault coverage); functional tests (532K cycles with 52% fault coverage); delay tests (15,232 patterns with 91% transition fault coverage); and SEMATECH I_{DDQ} tests (195 patterns with $> 96\%$ fault coverage). The SEMATECH experiment used $5\mu A$ as the I_{DDQ} pass/fail limit, which may not be good for production testing. In total, 18,466 devices were tested at the wafer level. A subset of them went through the other four test steps. Some additional characterization tests were also added to package-level tests. Test results were recorded for each test step and the kinds of tests failed were also marked. Since none of these four tests has complete fault coverage, one cannot simply say that a device that passes all four tests is realistically a perfect chip. What makes matters even worse is the single pass/fail current threshold of the I_{DDQ} test adopted. Therefore a device that failed only the I_{DDQ} test is not for certain defective, either. However, the subset of devices that went through several stages of burn-in and did not fail can give one some confidence. There is another kind of special case. Some devices failed at the wafer sort

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test stage, but passed all four tests after packaging or after some time at burn-in. Hence, the first research step is to clarify the classification standard. In this paper, these tested devices are categorized into three classes:

1. *Reliable good devices*, which are those passing all four tests in all five test steps, or passing all available test steps when not all steps are used. Devices that fail wafer probe test, but pass packaged test and burn-in, are counted here, because the error was due to poor wafer probe registration [11].

2. *Bad devices*, which include devices that failed the tests other than the I_{DDQ} test; or devices with extremely high I_{DDQ} current, say 450 μA, which it is believed will cause the chip to overheat after some time in use and then ruin it.

3. I_{DDQ} *only*, which failed only on the I_{DDQ} test with less than 450 μA I_{DDQ} current.

The statistical analysis is done based on this classification.

3 Previous Work

I_{DDQ} testing was first proposed in 1981 by Levi [6]. By the mid-1980's, I_{DDQ} test was recognized as an effective means to detect physical defects (bridging, gate oxide shorts, etc.) In the early 1990's, I_{DDQ} test gained commercial acceptance. In the mid-1990's, I_{DDQ} test was accepted as a cost-effective method (no overhead, few test vectors), and I_{DDQ} testing was correlated with reliability screening. In 1996, I_{DDQ} testing was identified by the Semiconductor Research Corporation to be one of the key testing methodologies for the late 1990's and beyond. I_{DDQ} testing methods can identify bridging faults, gate oxide shorts, a subset of delay faults, floating transistor gates, stuck-open transistors, leakage faults (punchthrough) and weak transistor faults. Most of these defects are due to resistive shorts between the four terminals of the transistor.

In prior work, there are two major categories of assumptions for the pass/fail criteria of a chip. The first assumption is that the variation range of the I_{DDQ} current measurement should be limited for a good chip. Gattiker and Maly [2] found that a significant break in the measured current in various vectors would happen in ordered I_{DDQ} measurements for a defective chip. Gattiker *et al.* [3] took a current measurement for the first vector, and rejected die based on subsequent vectors producing currents that differed from the first value by some threshold. Maxwell *et al.* [8] proposed a current ratio method, and used a statistical regression model to dynamically change the threshold according to different wafers and different processing. Thibeault [12] took differences in I_{DDQ} measurements between a vector and the next one to differentiate good and bad chips. According to Kruseman [5] these methods are effective for active defects [2] for up to 10 mA leakage current technologies, but they will miss passive defects.

The other assumption is that the absolute value of the I_{DDQ} current measurement should be less than a threshold. Henry and Soo [4] computed an I_{DDQ} mean for every vector, and rejected devices with any one I_{DDQ} measurement exceeding the mean of the corresponding vector. Li and McCluskey [7] sum up the total variances of I_{DDQ} current to check an I_{DDQ} curve with respect to the standard signature for all vectors. A DUT fails when the sum exceeds the mean by a certain value. Henry and Soo [4] and Li and McCluskey [7] take the *state dependence* into account, but they level out the *DUT dependence.* State dependence means that the I_{DDQ} current in a given logic gate depends on the input logic states of the gate. DUT dependence means that the I_{DDQ} current measured for a die depends on its position on the wafer. Kruseman *et al.* [5] assert that the DUT dependence will become dominate in deep submicron technologies. Sachdev [10] discusses options for deep-submicron I_{DDQ} testing, which include ΔI_{DDQ}, reverse body bias, and power-supply resistive drop methods.

4 New I_{DDQ} Classification Features

We first check the assumptions of prior models. For the first assumption, we plot each I_{DDQ} current versus test vector number for all 195 vectors on the current-vector axes, and call this the *band diagram.* Sample I_{DDQ} profiles for several chips are shown in Figures 1 through 11. Figures 1 and 6 are two kinds of good devices. There are 6,259 good devices out of 18,466 devices that have the form of Figure 6. Figure 9 represents a bad device. Any comparison of the means or variances will neither pass the chip of Figure 6 nor fail the faulty chip of Figure 9. Another 4,989 devices appear as in Figure 1, i.e., only one band. This also shows that there is no such thing as a current standard for each vector as the second assumption requires.

We can plot the I_{DDQ} profile in two ways, by points or by a line. Figures 1 and 2 show the profiles for the same device having a single-band profile. The faulty devices of Figures 3 through 5 also have single-band profiles, which only differ from those of good devices due to either continuous or spiked noise. The two-band I_{DDQ} profiles for a good device are shown in Figures 6 and 7. Two faulty two-band devices are depicted in Figures 8 through 11. The differentiation can only be made by the presence of noise in the band structure.

We propose the use of three new features of all I_{DDQ} current measurements for classification purposes:

- The number of bands that all of the current measurements cluster into,
- The width and separation of bands, and
- Current glitch detection among all I_{DDQ} measurements.

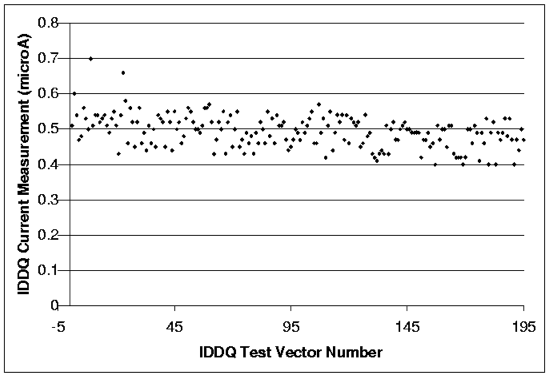

Figure 1: A good chip with a single-band I_{DDQ} (μA) profile.

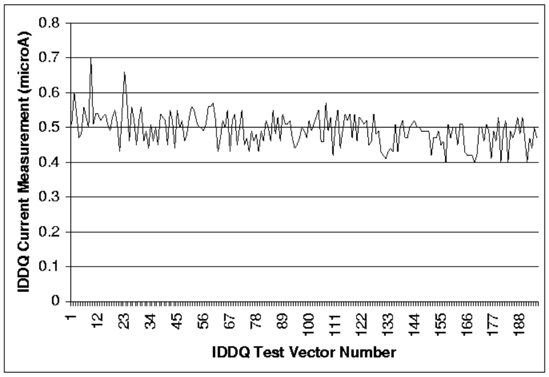

Figure 2: Alternative I_{DDQ} (μA) plot for the good chip of Figure 1.

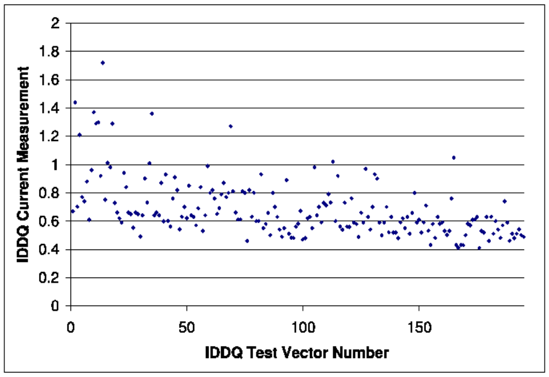

Figure 3: A faulty chip with smeared (noisy) single-band I_{DDQ} (μA) profile.

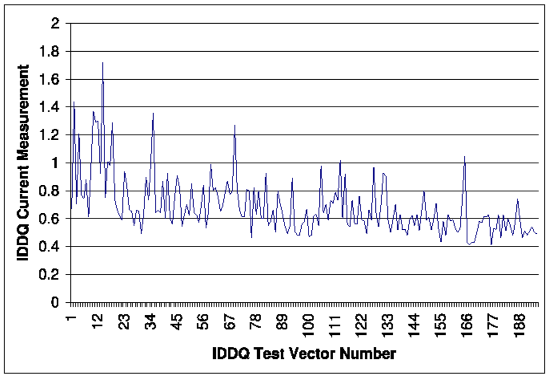

Figure 4: Alternate I_{DDQ} (μA) plot for the faulty chip of Figure 3.

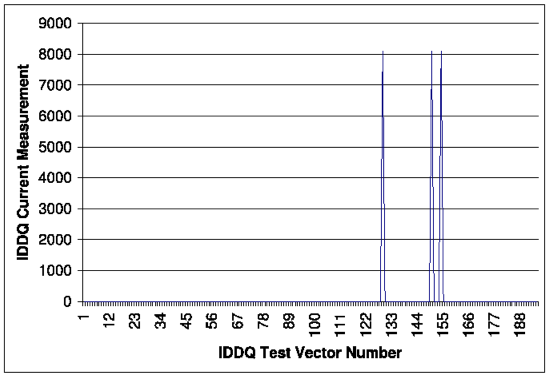

Figure 5: A faulty chip with a single-band I_{DDQ} (μA) profile having spiked noise.

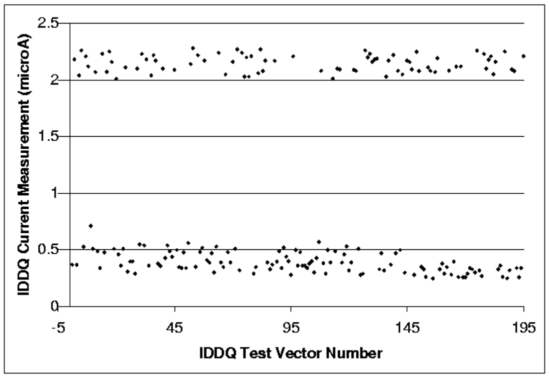

Figure 6: A good chip with I_{DDQ} (μA) profile displaying two bands.

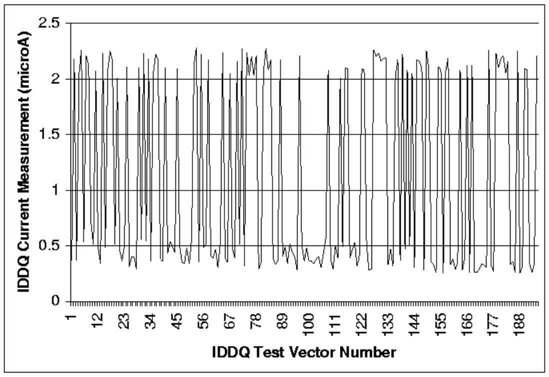

Figure 7: Alternative I_{DDQ} (μA) plot for the good chip of Figure 6.

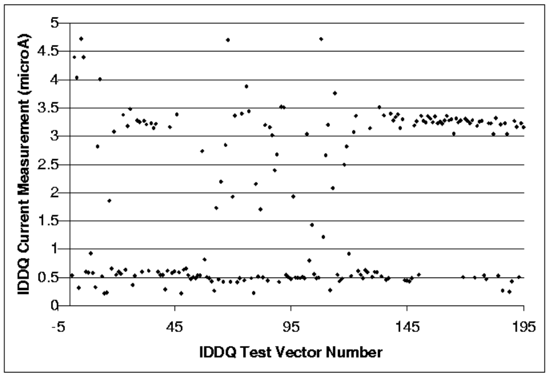

Figure 8: I_{DDQ} (μA) plot for another faulty chip with smeared two-band profile.

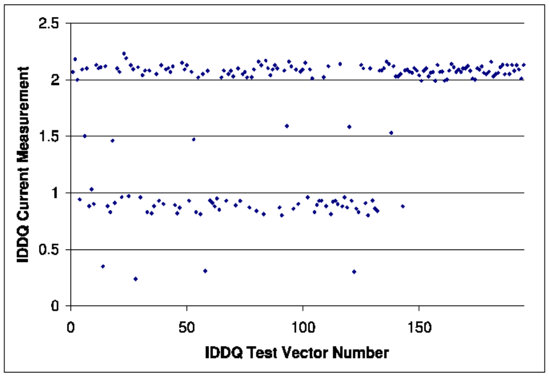

Figure 9: A faulty chip with smeared (noisy) two-band I_{DDQ} (μA) profile.

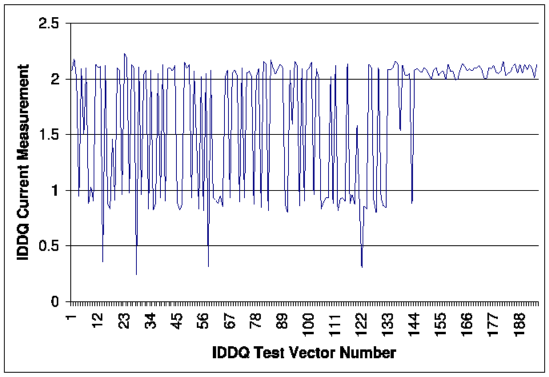

Figure 10: Alternative I_{DDQ} (μA) plot for the faulty chip of Figure 9.

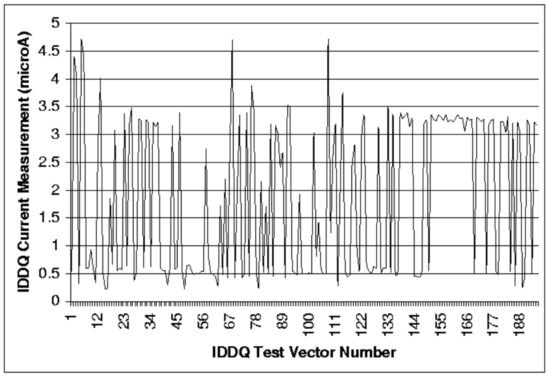

Figure 11: Alternative I_{DDQ} (μA) plot for the faulty chip of Figure 8.

Table 1: Band break statistics in SEMATECH data.

# Break	Good devices	Bad devices	Unknown devices
0	5684	1592	351
1	5674	2429	546
2	487	1144	104
3	12	367	31
>3	1	44	0

We found that even good devices often had I_{DDQ} measurements that clustered into well-defined bands as in Figure 6. Two or three bands in the good SEMATECH chips means that there are two or three different switching paths, possibly indicating a non-fatal bridging path(s) in combination with a lower defect resistance. This phenomenon may continue or worsen in deep submicron technologies.

Let us examine the statistics in Table 1 for all of the SEMATECH data, based on the classification standard of SEMATECH and IBM [9]. We chose $450 \mu A$ as the limit here to catch passive I_{DDQ} defects and because data analysis showed that any limit between $8 \mu A$ and $1 mA$ gave nearly the same result of lowest defect level. In addition to this criterion, if we relax the pass/fail current threshold to $450\ \mu A$, we also found from the SEMATECH test results and failure analysis data that:

1. If the device band diagram looks like Figure 8, which has unclear bands, then even if the number of bands is less than 4, the device is bad with more than 99% certainty. A possible explanation is that I_{DDQ} defects cause various bridging paths in the circuit. The bands become unclear because different vectors sensitize different paths, which leads to various different current measurements. This might explain why the bands smear and merge with each other.

2. If the band width is greater than $3.5\ \mu A$, then with more than 96% probability, the device is defective. The explanation of the band smearing (above) applies here.

3. If the bands, such as in Figure 6, part more than $5.1\ \mu A$, then it is more than 98% probable that the device is defective. This means that the shorting paths had lower resistance, so the difference in the current measurement between a vector that sensitizes a resistive short and one that does not increases.

4. If just a few points are far apart from the majority band, say 10 times the minimum current, as in Figure 5, then the device is more than 99% likely to be defective. The same physical explanation may apply as for the chips with widely-separated bands.

5. If the number of bands exceeds 3, as in Figure 9, then the device is 99% likely to be defective. The bands are determined by the Band differentiation algorithm, and the band width is then simply the difference between the maximum and minimum measurements put in this band by the algorithm. In this case, there are more than just two resistive shorting paths in the chip, so more bands appear, indicating a systematic problem with resistive shorting paths in this particular chip, and therefore a defective device.

```
Sort all $I_{DDQ}$ current measurements by value;
If two consecutive measurements differ by more than
    $10\% \times max(I_{DDQ})$ then
        { This is a band break;
        The higher band begins at the higher measurement;
        The lower band ends at the lower measurement;
        Increment the band break number; }
If the # bands $> 3$ then
    declare the chip as bad and exit;
else if max $I_{DDQ} > 450\ \mu A$ then
    declare the chip as bad and exit;
If any two bands are more than $5\ \mu A$ apart then
    declare the chip as bad and exit;
If (the 2nd or 3rd band is $> 6$ times wider than the 1st
    (lowest current level) band) or
    (any band extent $> 4\ \mu A$) then
    declare the chip as bad and exit;
```

Figure 12: Band differentiation algorithm.

```
Sort the entire set of 195 consecutive points by value;
If the maximum point differs from the 3rd maximum
    point by more than 10 times the minimum point then
        { Declare that a glitch exists;
        Declare the chip to be bad and exit; }
```

Figure 13: Glitch detection algorithm.

We can also connect the current points into one line. Figure 2 is typical of the majority of defect-free devices, i.e., a high frequency random waveform. Figures 4, 5, 10, and 11 are typical of the majority of defective devices. In Figure 5, obvious glitches are observed, while in Figures 4, 10, and 11, the waveform has high-frequency random signals. However, these three differ from Figure 7, as the amplitude changes obviously in some places. These irregular glitches can either be featured as different bands, or by observing glitches themselves. The changes in amplitude can be described by the number of bands, see Figure 9, which is the band diagram of Figure 10, or the unclear band, see Figure 3, which is the band diagram of Figure 4.

We now describe our new I_{DDQ} test result classifier, based on the above observations and the three new features. With proper correlation, the graphical I_{DDQ} evaluation criteria are set as follows:

1. If there are *unclear bands* existing in the band diagram, then the device is defective. Here unclear bands

Table 2: SEMATECH device statistics.

Total reliable functional devices	11858
Total # of unreliable devices	5576
Unknown devices	1032
Good pass number	11719
Bad pass number	333
Unknown pass number	153
Good fail number	139
Bad fail number	5243
Unknown fail number	879

Table 3: Summary of test escape and yield loss.

Good pass	Good fail	Bad pass
0.988278	0.011722	0.0597202
Bad fail	Unknown pass	Unknown fail
0.94028	0.148256	0.851744

mean that more than one group of data are clustered together; however, the edges are not clear and obvious.

2. If the band width is greater than 3.5 μA or if the bands part by more than 5.1 μA, the device is defective.
3. If the number of bands exceeds 3, then the device is defective.
4. If just a few obvious glitches are observed, then the device is defective.

One important matter in these criteria is that the exact number of the I_{DDQ} current measurements may not be the same for different designs, because the I_{DDQ} current relates to the manufacturing technologies and the size of the DUT, that is, how many gates are in the chip. These numbers can be obtained by observing a certain number of samples, with the help of voltage test methods.

We now summarize the method:

1. Analyze a representative sample of chips during characterization, and calculate (using a variety of tests) the # of bands, the band extents, the band separation, and the current glitch criteria for good chips to get a classification standard.
2. During manufacturing test, test each chip with the classification standard.

The *band differentiation* (Figure 12) and *glitch detection* (Figure 13) algorithms are a simplified implementation of the classification standard for SEMATECH data that accounts for measurement error.

Based on these criteria and the voltage test results, our DUTs are classified into 6 categories in Tables 2 and 3. They are described as follows.

1. *Good pass*: Those DUTs belonging to reliable functional devices that passed our evaluation.
2. *Good fail*: Those DUTs belonging to reliable functional devices that failed our evaluation.
3. *Bad pass*: Those DUTs belonging to unreliable devices that passed our test.
4. *Bad fail*: Those DUTs belonging to unreliable devices that failed our test.
5. *Unknown pass*: Those DUTs belonging to I_{DDQ} only devices that passed our test.
6. *Unknown fail*: Those DUTs belonging to I_{DDQ} only devices that failed our test as well.

5 Comparison and Discussion

No paper has given the total method statistics about the SEMATECH data except for the single threshold criterion, so we calculate the ΔI_{DDQ} results [12] from the IBM SEMATECH data. Table 4 compares the various I_{DDQ} methods on the SEMATECH data. I_{DDQ} methods compared include the single-threshold method and two kinds of ΔI_{DDQ} methods. The first ΔI_{DDQ} method uses 4 μA as the pass fail threshold for the current difference of two consecutive vectors, instead of 4σ, because 4 μA gave a much better yield loss rate. We also calculate the ΔI_{DDQ} method for 4σ, for comparison purposes, where σ is 0.35 μA, as given by Thibeault [12].

Table 4: Comparison of test escape and overkill in SEMATECH data.

Method	Test Escape	Overkill
Single-threshold	7.5%	2.3%
Current difference	35%	3.1%
ΔI_{DDQ} ($4 \mu A$)	8.6%	1.0%
ΔI_{DDQ} (1.4 μA, $\sigma = 0.35$)	7.6%	6.8%
Graphical I_{DDQ}	5.97%	1.2%

5.1 Reason for Yield Loss

All four test methods, Functional test, Delay test, Stuck-at fault test, and Single Threshold I_{DDQ} test, clearly do not provide complete fault-coverage on the SEMATECH data. Therefore, there is reason to believe that the super-low yield loss does not really mean too much, that is, these chips declared by the graphical method as defective may be realistically defective, although they have been declared defect-free by the other four testing methods. It is also undeniable that every method has some imperfection. The graphical method still cannot detect all defective DUTs.

Another reason may be that some defective chips may be stable but they may fail later in their lifetime.

5.2 I_{DDQ} Test Vector Selection

Since our goal is to let I_{DDQ} testing reduce the use of other test methods, one question is raised naturally by this result. Why are there still some missed defects? Can a purely I_{DDQ} test catch those missed defects? We analyze the effect of vector selection on I_{DDQ} defect detection. First where did the set of test vectors come from? The I_{DDQ} fault models are: stuck-at, pseudo stuck-at, bridging and special defects. The bridging fault model shows more efficiency than all others in detecting I_{DDQ} defects. It is commonly accepted that no single model can achieve complete I_{DDQ} fault coverage, so one should choose test vectors from all sorts of fault models. The correlation should be understood as not only statistical, but also physical. In the SEMATECH experiment, the I_{DDQ} test vectors consist of:

1. 125 vectors created by IBM's I_{DDQ} test generator, which targets pseudo-stuck-at-faults (95.7% fault coverage) (set # 1),
2. 10 vectors that applied simple, regular patterns into the scan chains (set # 2), and
3. The first 60 vectors of the stuck-fault tests (set # 3).

To verify the assumption that correlative selection of test vectors affects the fault-coverage, we also did experiments on a truncated set of test vectors. Table 5 gives the results. From these statistics, we can see that the 10 vectors (set # 2) that applied simple, regular patterns into the scan chains are more effective than the 60 stuck-at faults (the much longer set # 3) in terms of catching defects, given the number of test vectors added. We conclude that sets # 1 and # 2 are sufficient for testing. Randomly selecting test vectors does not work well in this method because of the information loss due to omitted vectors, but results show that increasing the number of randomly selected vectors improves test quality. Perhaps the graphical model still cannot catch all defects. A better solution may be the combination of multiple signatures. The experiment shows that a better selection of current measurement vectors leads to lower defect level.

5.3 How Reliable Is this Method?

It is well known that resistive opens causing a delay fault cannot be detected by conventional I_{DDQ} tests. With the graphical I_{DDQ} method, however, resistive opens causing delay faults can possibly be detected, because the open causes different switching paths compared to the good device, and hence slightly different I_{DDQ} currents flow. This phenomenon becomes more noticeable in deep submicron technologies.

Table 5: Test vector set truncation results.

Vector range	# Good devices out of 12,041	# Bad devices out of 5,545	# Unknown devices passing out of 880
# 1	11798	5210	144
# 1 + # 2	11804	5217	140
# 1 + # 3	11802	5214	134
# 1 + # 2 + # 3	11807	5218	130
50 random	11730	5155	182
100 random	11777	5190	161
140 random	11797	5196	149

Table 6: Devices escaping the graphical I_{DDQ} test.

Kind of failing voltage tests	Count / Total of kind
Stuck-at Failure Only	7/18
Delay Fault Failure Only	60/340
Functional Fault Failure Only	8/89
Fail functional test and delay test only	5/51
Fail stuck-at test and delay test only	29/54
Fail stuck-at test and I_{DDQ} test only	0/47
Fail functional test and I_{DDQ} test only	1/73
Fail functional test and stuck-at test only	37/78
Fail I_{DDQ} test and delay test only	5/85
Other 3 failed but not functional test	1/1234
Other 3 failed but not delay test	0/161
Other 3 failed but not I_{DDQ} test	35/90
Other 3 failed but not stuck-at test	0/18
All fail	0/3040
Short power fail	7/17

Table 6 gives the distribution of the sorts of DUTs that escaped the graphical I_{DDQ} test. On the other hand, there were nearly 200 chips that failed at the SEMATECH wafer-sort stage but afterwards passed all tests. Since these devices passed all four packaged tests, one can conclude that these are good devices with poor probing during the wafer probe test. Our results show that the graphical test would not have failed these 200 good devices. Since the classification algorithm can still be improved, we also recheck mis-judged bad chips visually using Microsoft Excel. We found another 105 chips that can be visually classified as bad using the criteria given in this paper, even though the above algorithm classified them as good. This additional classification would reduce the Test Escape percentage of the graphical test algorithm to 3.9%.

The efficiencies of all test methods and that of the graphical I_{DDQ} method are given in Table 7. It is obvious that the graphical method identifies more defective chips

Table 7: Comparison of efficiencies of test methods.

Kind of test method	% Defective chips detected
Functional Test	65.0 %
Stuck-at Test	85.1 %
Delay Test	88.5 %
I_{DDQ} Test	87.0 %
Graphical I_{DDQ} Test	96.1%

than other methods. The graphical method also has lower yield loss, because of the 200 chips that first were declared bad but later turned out to be good under the SEMATECH methods. Many of these chips probably had misregistered probes during wafer test, and therefore were actually good.

6 Conclusion

We proposed a new way to look at I_{DDQ} current, using a graphical evaluation method. We showed that this method can catch some defects that other I_{DDQ} tests cannot. This fact puts the conventional belief that I_{DDQ} testing cannot partially replace voltage tests into doubt again. This graphical I_{DDQ} test may substantially reduce the volume of conventional voltage tests and burn-in effort. This method has slightly higher yield loss than others. These losses may not really be losses, since the tests are incomplete.

We clearly define the device classes, and did exhaustive experiments on the IBM SEMATECH data. The results show promising signs that I_{DDQ} testing can still survive through deep submicron technology, because this method does not relate results of I_{DDQ} testing to absolute current measurements, but rather to the shape of the series of measurements.

The computational complexity of the graphical method is $O(n \log n)$, since the most computation-intensive part is sorting. This method gives more clear insight, more realistic criteria, and hence it can catch more defects, i.e., it has a lower defect level. This technique can be easily adapted to existing *automatic test equipment*, because it is programmable and can store current measurements.

Further research can be done using test vectors generated from multiple fault models, and physical diagnosis needs to be done on those devices that caused yield loss. More features of defective devices need to be found for the I_{DDQ} test to replace other tests. When the fabrication process changes, the band differentiation and glitch detection algorithms must be changed to reflect the changed features of defective chips.

Acknowledgement

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