Fault Collapsing via Functional Dominance

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Abstract

A fault f_j is said to dominate another fault f_i if all tests for f_i detect f_j. When two faults dominate each other, they are called equivalent. Dominance and equivalence relations among faults around a Boolean gate are called "structural" and are used for fault collapsing in large circuits. Some fault equivalences, that cannot be determined by the structural analysis, can be found by "functional" equivalence relations. This paper gives a "functional dominance" relation, which has not been described in the literature. Since the functional analysis is computationally expensive, it can only be applied to small circuits such as standard cells. A graph-theoretic hierarchical fault collapsing method from the recent literature can then collapse faults in any large cell-based circuit. It is found that the size of the dominance collapsed set for an exclusive-OR cell reduces to just four faults when functional dominance is considered. With the traditional method of structural collapsing this set contains 13 faults. When the exclusive-OR cell is used to build an 8-bit adder circuit, the size of the dominance collapsed set reduces to 112 faults from a total of 466 faults. Traditional structural dominance collapsing would have given a set of 226 faults. Smaller fault set can lead to more compact tests. Collapsing for the cell-based design of benchmark circuit, c499, reduces a set of 2,710 faults to just 586 faults.

1. Introduction

Fault collapsing is considered a matured topic and is discussed in text-books [1, 6]. Collapsing reduces the number of faults to be considered in test generation and fault diagnosis and is routinely incorporated in test generation and fault simulation programs. The techniques used are termed "structural" fault dominance and fault equivalence, which can reduce the fault set size by about 50%. Greater reduction is possible with "functional" techniques, which, due to high complexity, can only be applied to small circuits. They have not been used in practice. A recent method applies functional equivalence collapsing at the cell-level and then uses the result for hierarchical fault collapsing in large circuits [15].

While functional equivalence has been known for a long time, functional dominance, though mentioned in the literature [11, 12], has not received much attention. This paper redefines functional dominance and illustrates its application in hierarchical fault collapsing.

Main Contribution: A quick reading of this paper may show similarities to our recent ITC'02 paper [15]. Indeed, the hierarchical method of fault collapsing described in that paper is used here. The details of that method are not included here. The ITC'02 paper illustrates the application to functional fault equivalence. The topic of this paper is *functional dominance* and its application to fault collapsing. We believe the procedures given here are different and more effectively implemented than those given by Al-Assad and Lee [4], Amyeen *et al.* [5], Grüning *et al.* [8], and Lioy [11, 12]. Also, the demonstration of the reduction of the collapse ratio below 25% by using functional dominance is significant and has been observed for the first time.

2. Known Results

We will first summarize the known results on fault collapsing that form the background for the new result of this paper, discussed in the following sections. The background material given in this section can be found in any text-book on testing [1, 6] and in the cited references.

2.1. Structural Equivalence and Dominance

Two faults are called *equivalent* if exactly the same set of tests detect them. These faults are *indistinguishable* from each other. Single stuck-at faults at the inputs and output of a Boolean gate have *structural* equivalence relations. For example, all stuck-at-0 (s-a-0) faults of the input and output lines of an AND gate are equivalent. Similar structural equivalence relations are available for other gates. Using these relations, faults of a circuit are grouped into sets of equivalent faults. One fault is then selected from each equivalence fault set to form an *equivalence collapsed set*, which is used for test generation and fault coverage measurement. This process of reducing the fault set is known as *equivalence fault collapsing*.

Another type of fault collapsing is based on fault dominance [1, 6]. A fault is said to dominate another fault if all tests for the second fault detect the first fault. For example, a s-a-1 fault on the output line of an AND gate dominates a s-a-1 fault on any input line of that gate. This kind of dominance relations across Boolean gates are known as *structural dominances* and are used to find dominance collapsed fault sets. Tests that detect all faults in a dominance collapsed set also detect all testable faults of the circuit.

As an example, the test generation program, Hitec [13], produces an equivalence collapsed set of 1,574 faults for the benchmark circuit c1355, which has a total of 2,710 faults. Another program, Fastest [10], finds a dominance collapsed set of 1,210 faults. Both programs use structural collapsing.

2.2. Functional Equivalence

For an input vector, V, to be a test for a fault, we have

$$f_0(V) \oplus f_1(V) = 1 \tag{1}$$

where f_0 is the fault-free function and f_1 is the faulty function, respectively. Consider a second fault that produces a faulty function f_2. According to the definition of fault equivalence, two equivalent faults have exactly the same tests. Therefore, for two faults to be equivalent, we have

$$[f_0(V) \oplus f_1(V)] \oplus [f_0(V) \oplus f_2(V)] = 0 \tag{2}$$

Manipulation of the above equation leads to the following result:

$$f_1(V) \oplus f_2(V) = 0 \tag{3}$$

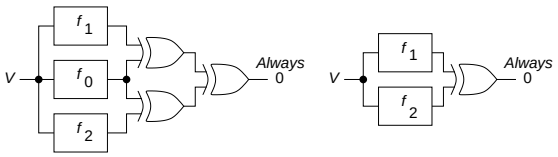


Figure 1: Two ways to view fault equivalence.

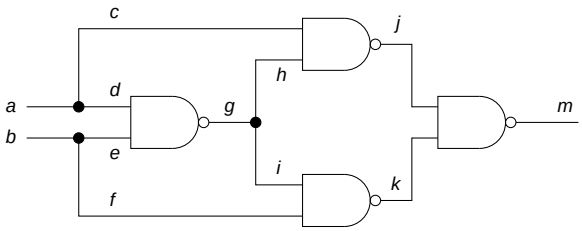


Figure 2: An *xor* cell.

which means that the two faulty functions are identical. This is the most general definition of fault equivalence and is known as *functional fault equivalence* [6]. Equations 2 and 3 are functionally depicted in Figure 1.

Consider the exclusive-OR cell shown in Figure 2. It has a total of 24 single stuck-at faults that can be reduced to an equivalence collapsed set of 16 faults if we use the structural collapsing as outlined in the previous subsection. All equivalences, both structural and functional, as shown in Table 1, can only be found when either exhaustive fault simulation or symbolic analysis of faulty circuits is performed. Here we have used subscripted notation for faults. Thus, a_0 is the fault "line a s-a-0." Functional equivalences, that cannot be identified structurally, are shown in "double-quotes." Taking one fault from each equivalent set, we get a collapsed set of 10 faults. This set is smaller than the set of 12 faults found in a previous paper [15] since the functional equivalences in sets 5 and 8 were not identified there.

The result of Table 1 first appeared in the papers by Lioy [11, 12], who proposed functional fault collapsing based on *D-frontiers* used in the automatic test generation (ATPG) procedures of Roth *et al.* [16]. Proving the equivalence of two faulty circuits is another possible way of identifying functional equivalence. Efficient methods of proving equivalence have been used by Grüning *et al.* [8] and Amyeen *et al.* [5]. High

Table 1: Equivalent fault sets for *xor* cell.

Set No.	Equivalent faults	Faulty function
1	a_0	b
2	a_1	$\overline{b}$
3	b_0	a
4	b_1	$\overline{a}$
5	c_0, "e_1", h_0, j_1	$\overline{a}b$
6	"c_1", "f_1"	$\overline{ab}$
7	d_0, e_0, g_1, "h_1", "i_1"	$a+b$
8	"d_1", f_0, i_0, k_1	$a\overline{b}$
9	"g_0", "m_0"	0
10	j_0, k_0, m_1	1

complexity still prohibits application to large circuits. Al-Assad and Lee [4] give a simulation-based procedure for finding global equivalences in large circuits. However, their method is approximate and may fail to find many equivalences.

In practice [10, 13], functional equivalences are not used due to the high complexity of analysis. We also do not suggest direct identification of functional equivalences in a large circuit. However, the result of small subnetworks can be used to advantage if hierarchical fault collapsing is adopted [15]. Once the fault equivalences of small cells are given, collapsing in large circuits can be performed by using a transitive closure graph. Although some global functional equivalences may not be found, the effects of cell equivalences are globally analyzed.

Consider c499, which contains 104 exclusive-OR gates. If each exclusive-OR gate is replaced with the four-NAND *xor* cell of Figure 2 then we obtain a circuit that is functionally and structurally identical to c1355. We will call this expanded version of c499 as c499exp. Similar to c1355, c499exp has a total of 2,710 faults and conventional techniques produce an equivalence set of 1,574 and a dominance set of 1,210 faults. When we consider the functional equivalences for the *xor* cell, the hierarchical fault collapsing [15] provides an equivalence set of 950 faults and a dominance set of 690 faults. These numbers are lower than those published for c499exp in an earlier paper [15]

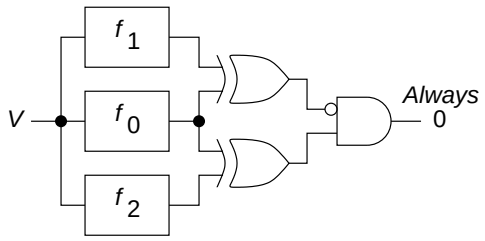


Figure 3: Fault dominance.

because some functional equivalences of the *xor* cell were not used there.

3. Functional Dominance – New Result

Consider again two faults, which produce faulty output functions $f_1(V)$ and $f_2(V)$, respectively, where V is an input vector. Extending the concept of functional equivalence Abramovici *et al.* [1] define fault dominance: If a fault f_1 dominates the fault f_2 then the two faults are functionally equivalent for the input vector set that tests the fault f_2, i.e., all tests of f_2 satisfy Equation 3. To define the *functional dominance* we will derive an equation involving the two faulty functions and the fault-free function that must be satisfied by all input vectors.

Let the fault-free output be denoted as $f_0(V)$. Any vector V that detects the first fault must satisfy Equation 1. Similarly, if V is a test for the second fault, then it must satisfy:

$$f_0(V) \oplus f_2(V) = 1 \tag{4}$$

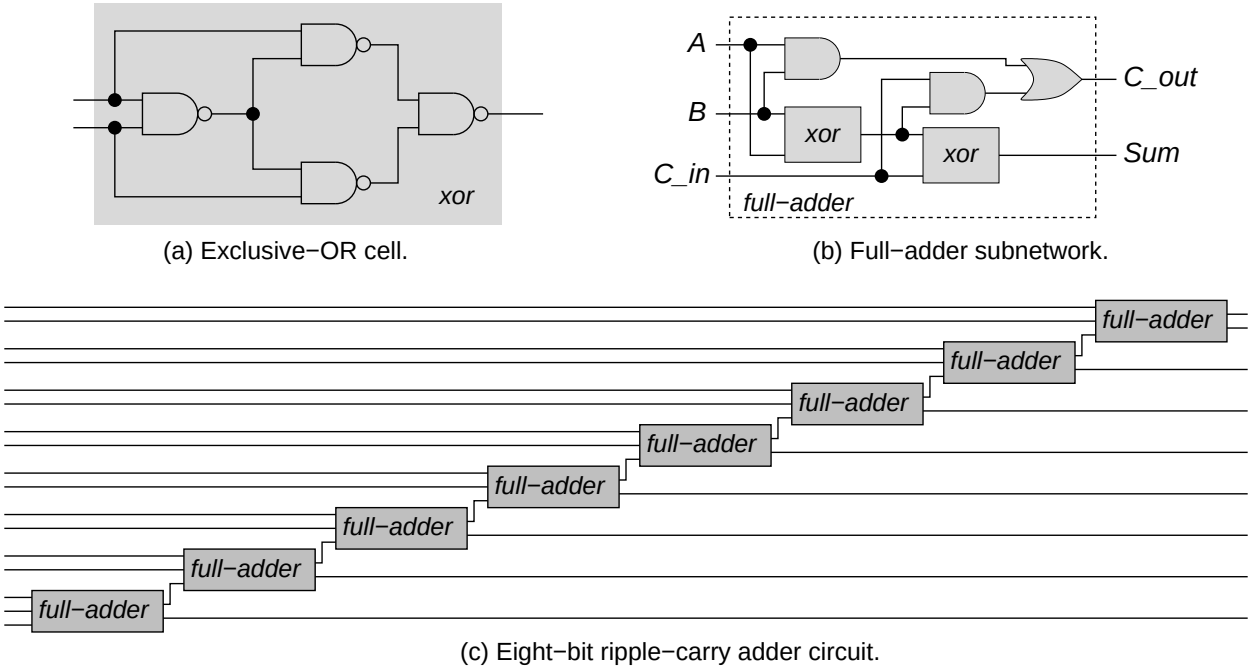
If the first fault dominates the second fault then any vector that satisfies Equation 4 must satisfy Equation 1. Also, by contra-positive law, any vector that does not satisfy Equation 1 must not satisfy Equation 4. These conditions are combined in the following equation that must be satisfied by all input vectors:

$$[f_0(V) \oplus f_2(V)]\overline{[f_0(V) \oplus f_1(V)]} = 0 \tag{5}$$

This relation is depicted in Figure 3. Equation 5 reduces to:

$$\overline{f_1(V)}f_2(V)\overline{f_0(V)} + f_1(V)\overline{f_2(V)}f_0(V) = 0 \tag{6}$$

Although it is not obvious, this condition is consistent with the D-frontier representation of functional fault dominance given by Lioy [11, 12]. We



(a) Exclusive−OR cell.

(b) Full−adder subnetwork.

(c) Eight−bit ripple−carry adder circuit.

Figure 4: Hierarchical design of an 8-bit ripple-carry adder.

re-examine the circuit of Figure 2, which is small enough for the application of Equation 6. We find many non-obvious dominances, such as, j_0 dominates d_0, and g_0 dominates k_1. This circuit has 24 faults and all of the pair-wise dominances are represented as a 24×24 *dominance matrix* of [0,1] elements as described by Prasad *et al.* [15]. The transitive closure of this matrix then provides additional global dominances. Analyses of the transitive closure provide equivalence and dominance collapsed fault sets. The reader is referred to a recent paper for the details of this technique [15].

When we obtained all pairwise dominances from Equation 6 and used the dominance matrix method [15], the equivalence collapsed set had 10 faults: a_0, a_1, b_0, b_1, c_0, c_1, d_0, d_1, m_0, m_1, and the dominance collapsed set had four faults: c_0, c_1, d_0, d_1.

The 10-fault equivalence collapsed set is consistent with Table 1, which was obtained using functional equivalence. Here this set is obtained by the use of functional dominances. We should point out that dominance is a more basic property than the equivalence. If two faults dominate each other, then they will be equivalent. Thus, when all dominances are known all equivalences can be deduced. The converse is not always true.

These are smallest possible equivalence sets. We notice that coincidentally the four faults in the dominance collapsed set are *mutually independent*. Two faults are called independent if they do not have any common test [3]. In this case the four faults give the exhaustive set of four vectors. Derivation of independent fault sets is an open problem.

4. Hierarchical Fault Collapsing Results

Figure 4 shows an eight-bit ripple-carry adder circuit with three levels of hierarchy; first level is the *xor* cell, second level is the full-adder subnetwork containing the *xor* cell, and the top level is the ripple-carry adder circuit. The circuit consists of eight full-adder subnetworks, which are constructed with *xor*, AND and OR cells.

Once again, the reader is referred to the recent ITC paper [15] for the graph-theoretic method of hierarchical fault collapsing that we have used in this example. In that method, dominance matrices for all standard cells are obtained by taking all structural and functional dominances. Since a cell is small, exhaustive simulation or symbolic analysis is possible. Our cell library for this example consists of the reduced (collapsed) dominance matrices for *xor*, AND

Table 2: Fault collapsing results.

Circuit name	All faults	Number of collapsed faults (Collapse ratio [6])					
		Structural only		Functional equivalence		Functional dominance	
		Equivalence	Dominance	Equivalence	Dominance	Equivalence	Dominance
xor cell	24	16 (0.67)	13 (0.54)	10 (0.41)	8 (0.33)	1 0 (0.41)	4 (0.17)
full-adder	60	38 (0.63)	30 (0.50)	26 (0.43)	20 (0.33)	26 (0 .43)	14 (0.23)
8-bit adder	466	290 (0.62)	226 (0.49)	194 (0.42)	156 (0.34)	194 (0.42)	112 (0.24)
c499exp	2710	1574 (0.58)	1210 (0.45)	950 (0.35)	690 (0.26)	950 (0.35)	586 (0.22)

and OR cells. Similarly, fault collapsing libraries can be made for any set of standard cells. We first analyze the full-adder subnetwork using the reduced dominance matrices from the cell library. Using the transitive closure, we reduce the dominance matrix of the subnetwork. Next, eight copies of this reduced matrix are combined for the ripple-carry adder. In this way, the entire circuit is never flattened and the full-adder subnetwork data, analyzed once, is repeatedly reused. Also, functional fault dominances, incorporated in the *xor* cell, are automatically used in the analysis of the larger circuit. However, to avoid high complexity, some functional dominances that may be present in the full-adder subnetwork or in the 8-bit adder are ignored.

These results are shown in Table 2. Sizes of collapsed fault sets and *collapse ratios* are given. The latter is defined as [6]:

$$\text{Collapse ratio} = \frac{|\text{Set of collapsed faults}|}{|\text{Set of all faults}|}$$

A collapse ratio around 0.6 is quite typical of the conventional structural equivalence collapsing. It is about 0.5 for structural dominance collapsing. However, functional dominance collapsing, which is the main topic of this paper, reduces the collapse ratio to below 0.25 (see the last column in Table 2).

The flat fault collapsing is conventional and is done by flattening the hierarchy to the Boolean gate level. The total number of faults, listed as "all faults" is counted at this level. Collapsing in this case is structural only. Equivalence collapsed faults were obtained by ATPG programs, Gentest [7], Hitec [13] and Fastest [10], all of which gave identical results. Dominance fault collapsing numbers were obtained from Fastest. The same equivalence and dominance numbers were obtained when the graph method was applied to the flat gate-level circuits.

Hierarchical fault collapsing, both equivalence and dominance, were done by the graph method with "functional" equivalences incorporated in the *xor* cell [15]. The total number of faults remains the same as that at the flat level. Functional equivalences provided smaller collapsed fault sets and we observed a 35% reduction in the CPU time over that needed for collapsing at the flat level. The collapsed set sizes in columns 5 and 6 of Table 2 are smaller than those previously reported [15] because two of the five functional equivalences (see Table 1) were ignored there.

The last two columns in Table 2 give the new result of this paper. Most commercial ATPG tools use structural equivalence collapsing and will therefore have 290 faults for the 8-bit adder circuit. This number is reduced to 112 by the functional dominance collapsing.

The last row in Table 2 gives the results for the c499exp circuit discussed in Section 2. Once again, the numbers for functional equivalence are lower than those reported in an earlier paper [15] because all functional equivalences of the *xor* cell are considered here. The results for functional dominance are being reported for the first time.

We performed a test generation experiment using Gentest [7]. Tests for 100% coverage were generated for the 8-bit adder using the collapsed sets of 290 faults (conventional) and 112 faults (functional dominance). We used several modes available in Gentest that either leave the don't care inputs of a test as such, or fill them by 0, 1, or random bits, respectively, before fault simulation for dropping other detected faults. The results, as shown in Table 3, though not dramatic, distinctly show that the functional dominance collapsing does reduce the test set size. For circuits with greater logic depth, we should expect larger reduction in test vectors.

We should point out that even the smallest test

Table 3: 100% fault coverage tests for 8-bit ripple-carry adder.

Fill mode	Number of vectors generated from	
	290 faults	112 faults
don't care	65	49
0s	35	31
1s	32	27
random	16	13

set in Table 3 is not minimal. There are ATPG programs [14] that try to construct small test sets from any given fault list. Besides, considering the repeated structure of the ripple-carry adder it is found that all faults can be covered by eight or fewer vectors [6]. In general, the smallest test set is found by an ATPG program if an independent set of faults is targeted [3]. In such a fault set no two faults are detectable by the same vector. Although we notice that the set of four faults found by dominance collapsing in the xor cell is an independent set, in general, the collapsing procedure does not produce an independent fault set. This is because it is possible to have a common test for certain fault pairs where neither of the two faults dominates the other. When the dominance collapsed set contains such a fault pair, one must find a *concurrent test* for it. A concurrent test for two faults is a single test that detects both faults. These topics require further investigation.

5. Conclusion

When functional fault dominances are used, the sizes of both equivalence and dominance collapsed sets reduce. The concept of fault dominance is more general than fault equivalence and leads to an elegant graph-theoretic analysis [15]. The advantage of functional dominance collapsing in reducing the test length, though not too significant for the example of 8-bit ripple-carry adder, can be large for circuits with deep logic levels. Another possible application is in identifying sets of independent faults. Such faults have disjoint sets of tests and their use in test generation provides the smallest possible test sets [3].

The use of dominance fault collapsing for ATPG requires caution. It is known that when a dominated fault in the collapsed set is found to be redundant, the dominating fault (not included in the collapsed set) can be testable [2]. Thus, unless at least one of the dominated faults is tested the dominating fault cannot be considered as covered.

In general, smaller collapsed fault set can improve the diagnostic resolution in fault diagnosis. This is because it is impossible to distinguish between equivalent faults. Such applications, which generally use equivalence rather than dominance collapsing, have been discussed by Hartanto *et al.* [9].

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