On the Guaranteed Failing and Working Frequencies in Path Delay Fault Analysis*

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Abstract

When running a set of test vectors to detect path delay faults in a digital system, desired test frequencies are needed. In this paper we determine the guaranteed failure frequency (GFF) and the guaranteed working frequency (GWF) for a given set of test vectors used for path delay testing of a sequential circuit. If the circuit passes the test when the vectors are applied at GFF, then all paths activated by those vectors are guaranteed to be free from delay faults provided the clock frequency does not exceed the GWF. Ambiguity cancellation and minmax-delay or statistical-delay modeling techniques are used in a timing simulation system to determine GFF and GWF. Experiments show that by using the guaranteed failure frequency, we can obtain the best (most reliable) path delay fault coverage provided by the given test vectors.

1 Introduction

Failures causing logic circuits to malfunction at desired clock rates are called delay faults or AC faults [10, 12]. There are several delay fault models, including gate delay, path delay, and transition delay. A path delay fault is referred to as the inability of a given path to propagate signal changes within the system clock window.

Information on existing delay test techniques and capabilities may be found in the literature [6, 8, 10, 12]. Computation of appropriate clock frequencies for path delay fault testing in combinational and sequential circuits is crucial for its adoption as an acceptable screening vehicle. In a recent paper [5], a definition of the *guaranteed failure frequency* (GFF) for path delay test application was given.

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In this paper, we provide experimental evidence that a properly chosen test frequency will most likely result in the achievement of a nearly optimal delay fault coverage that is possible with the given test vectors, while maintaining a close to maximum manufacturing product yield.

The guaranteed failure frequency (GFF) is the lowest clock frequency above which the circuit is guaranteed to fail when a delay fault exists on any path that is testable by the given vectors.

We have implemented a selective hazard suppression technique for the calculation of such frequency. Timing simulation is used to achieve this frequency. The method employs ambiguity delay simulation techniques to implement event cancellation for hazard suppression. Also, the minmax or statistical information on delays is used.

The guaranteed working frequency (GWF) is the highest operating frequency below which the circuit operation is guaranteed to be error-free with respect to all paths tested by the given test vectors applied at the GFF.

Delay faults that might potentially exist in the circuit will not *disturb* its logic function at low clock rate. By definition, a "grey" window exists between the frequencies GWF and GFF: in this region not all targeted path delay faults are detectable, and the circuit can potentially fail in operation even after it has passed the tests. If all tests are robust, then the two frequencies will be identical. However, in general, some paths are only non-robustly tested. The GWF, in that situation, should be suitably lowered for a guaranteed correct operation.

Suppose, a two-pattern delay test is applied to the circuit shown in Fig. 1. Assuming that each gate has a propagation delay of 1 unit, the output response experiences a dynamic hazard, details of which are shown in Fig. 2. Notice that for all output strobes at clock frequencies greater than GFF the test will definitely show

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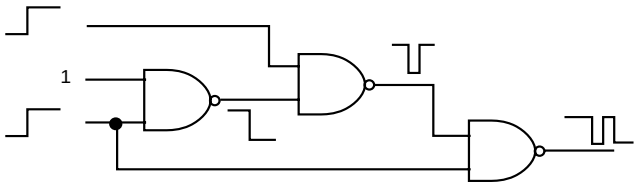

Figure 1: A possible circuit response to a delay test

a failure. At frequencies below GWF the test will produce a correct output. At frequencies between GFF and GWF the test result may be ambiguous because of the hazard. For a hazard-free test GFF and GWF will be arbitrarily close. Notice also that the transition at time $t = 1$ is produced by the shortest path. The transition at time $t = 3$ is produced by the longest path. Accurate determination of GFF and GWF can be performed by a timing simulator.

In general, gate-delays cannot be assumed to be fixed. They vary from circuit to circuit due to variations in the manufacturing process. Some common ways of modeling delays are:

- Nominal delays – Each gate is assumed to have lumped *rise* and *fall* delays, computed from transistor and gate loading characteristics.
- Minmax delays – Minimum and maximum delays are estimated for each gate from device characteristics and process variation data.
- Statistical delays – The delay for each gate is estimated as a statistical variable with mean (μ) and standard deviation (σ).

Techniques exist for the simulation of any of the above types of delays. For our experiments, we use unit-delay, minmax-delay, and statistical-delay. In the two latter cases, the simulator produces an *ambiguity region* in place of the detailed transient waveform as shown between time units 1 and 3 in Fig. 2. The gap between GFF and GWF occurs due to the ambiguity region in which dynamic or static hazards can be expected. Our studies show that an imprecise evaluation of frequencies GFF and GWF will either over-optimize the product yield (by overriding some detectable delay faults), or make the testing results too pessimistic (by not taking credit for some of the detectable faults). A digital simulation system that supports ambiguous delay modeling is used in our experiments.

Bose *et al.* [5] propose an event cancellation algorithm to suppress hazards for the purpose of estimating the failure frequency from maximal path delay variations. We improve that method by adding the two techniques mentioned earlier: the common ambiguity cancellation

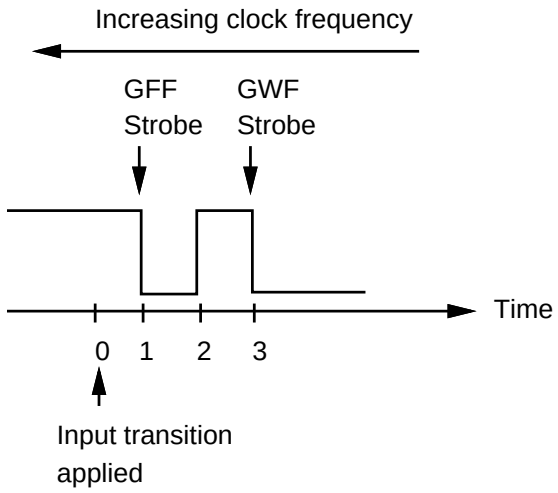

Figure 2: Output response of the circuit of Fig. 1 with unit-delay gates

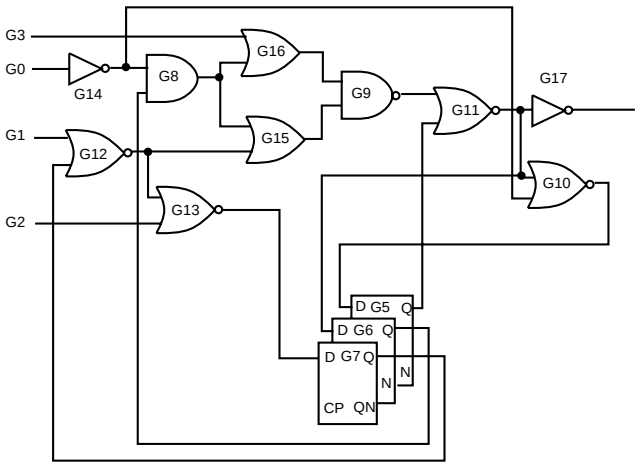

Figure 3: S27 circuit diagram

technique and the minmax or statistical timing specification technique. We use capacitance and driver delay information to calculate the real circuit library cell delays. This cell delay database and the above implemented techniques constitute the needed data and methodology for determining the GFF and GWF frequencies.

2 Illustrative Example: S27

Consider the ISCAS'89 benchmark circuit [7], S27, shown in Fig. 3. Physical paths can be categorized into four distinct classes:
Primary inputs to primary outputs (PIs to POs)
Primary inputs to latch inputs (PIs to QIs)

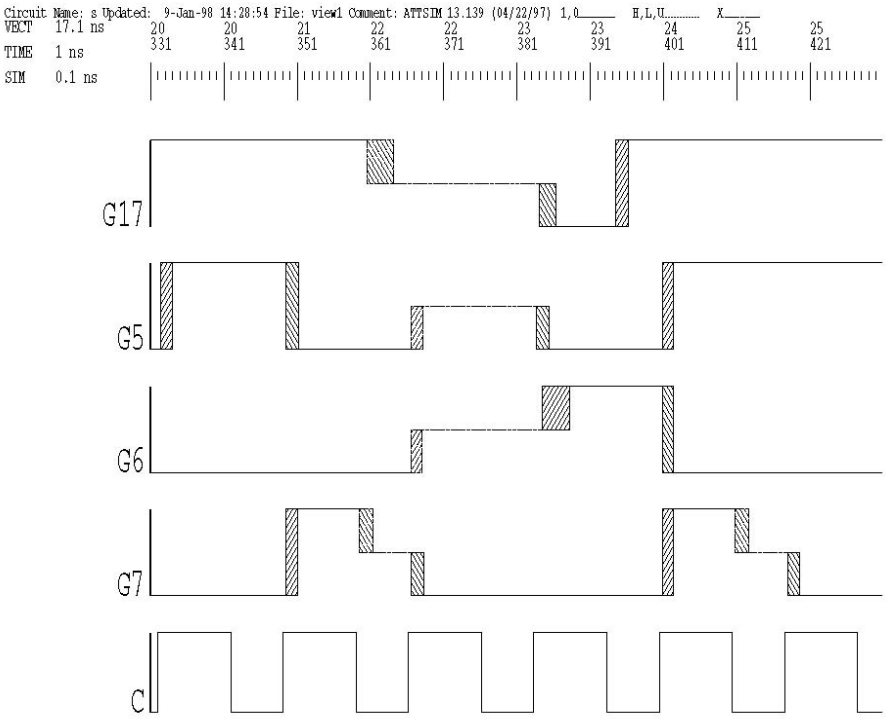

Figure 4: Typical waveforms for S with deterministic vectors

Latch outputs to primary outputs (QOs to POs)
Latch outputs to latch inputs (QOs to QIs)
These categories are referred to as A, B, C, and D, respectively. For S27 we have the following:

PIs: G0, G1, G2, G3
POs: G17
QIs: G10., G11, G13 QOs: G5, G6, G7

Examples of paths:
Category A: G0 → G14 → G8 → G16 → G9 → G11 → G17
Category B: G0 → G14 → G10 → G5
Category C: G5 → G11 → G17
Category D: G5 → G11 → G10 → G5

Traditional path delay analysis requires the evaluation of the longest physical path in order to determine the GWF. Since, not all physical paths are functional, ideally, the GWF should be selected from the set of all *functionally sensitizable* paths. The longest functionally sensitizable path is sometimes referred to as the *critical path.* Every functionally sensitizable path needs to be tested for both *slow to rise* (STR) and *slow to fall* (STF) signal transitions. The propagation delays for these two events are normally different. In our analysis, we will obtain GFF and GWF only for the longest path that is sensitized by the given test vectors.

For S27 we use two types of test vectors: a deterministic test set and a randomly generated set of vectors with 0.5 input signal probabilities.[1] The deterministic vectors were obtained from a sequential circuit test generation program, *Gentest* [1, 3].

Fig. 4 shows portions of timing waveforms that resulted from the application of the set of deterministic vectors to S27. This result was obtained by a timing simulation program, *ATTSIM* [2]. Simulation was done in the *minmax-delay* mode [4], using the 0.9-micron CMOS library of Lucent Technologies. Vectors are applied to primary inputs at the rising edge of the clock signal (C). Primary output (G17) and flip-flop signals (G5, G6 and G7) are shown in Fig. 4. The shaded portions are the ambiguity regions in which possible transients might occur. When the clock period decreases below 10.9 ns some unknown signals appear. These are shown as values half-way between "high" (logic 1) and "low" (logic 0) values. The first mismatch at the primary output occurs on vector number 22, and is caused by an incorrect value in G7. Thus, GWF corresponds to a clock period of 10.9 ns.

[1] The signal probability of a line is the probability that the line will carry a value 1.

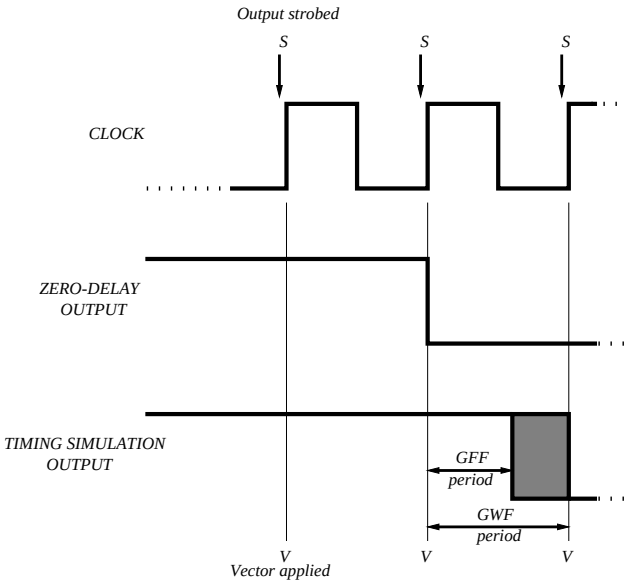

Figure 5: Simulation output analysis for determining GWF and GFF

The procedure for determining GWF and GFF is illustrated in Fig. 5. This procedure first requires a zero-delay simulation. All combinational gates are assumed to have zero-delay and flip-flops are synchronously clocked with a non-zero period. Vectors are applied at the beginning of each clock period (instants shown as V in Fig. 5) and primary outputs are strobed just before the end of the period (instants S). Since the gates have no delay, irrespective of the clock frequency, correct logic values are obtained for all signals.

Next, the simulation is repeated using the selected timing mode (minmax-delay for the present example). Starting from a large clock period, where the results match with the zero-delay output, we repeat the simulation successively reducing the clock period until a mismatch occurs. In general for the timing mode, the logic transitions have the ambiguity regions (shown as shaded area in Fig. 5). Since we are reducing the clock period from a large value, the first failure occurs due the longest delay path that is sensitized by the vectors. This period corresponds to GWF. For the failing output, if we subtract the width of the ambiguity region from the clock period, we get the period of GFF. If the circuit has multiple outputs, notice that the GFF is the test frequency for that specific output where the failure is observed. The GWF, of course, is a valid operating frequencies for all outputs of the circuit.

Table 1 shows the measured values for GFF and GWF for S27 using both deterministic and 1,000 random vectors. Notice that the table entries are actually clock periods and not clock frequencies. Obviously, the results are only as good as the patterns being supplied. A "good" set of patterns should exercise all critical paths. If some critical paths are missed the results cannot be considered reliable. In general, the computed GFF and GWF are functions of test vectors, the component delays, and the circuit topology.

Table 1: Clock periods for GFF and GWF for S27

Vectors	GFF (ns)	GWF (ns)	Failing Vector
Determin.	8.0	10.9	21–22
Random	11.2	12.9	173–174

It is evident that random vectors tested longer paths in this case. Perhaps more vectors in the random set (1,000 versus 30) may have provided greater opportunity to activate some longer paths. In fact, none of vector sets actually targeted any paths, specifically.

3 GFF and GWF Evaluation

Our evaluation of GFF and GWF is based upon Lucent Technologies' ATTSIM 3.5 [2], mixed-mode (analog and digital) timing simulation system. The simulator was used in unit-delay, minmax-delay and statistical-delay modes, in addition to the zero-delay simulation. The circuits were modeled using the 0.9-micron CMOS library of Lucent. The simulator extracts the minimum (d_{min}) and maximum (d_{max}) delays for all gates. Simulation algorithms for the minmax-delay mode are described by Bierbauer *et al.* [4].

In the statistical-delay mode, each gate is modeled with a Gaussian *gate-delay distribution* for which the mean (μ) and standard deviation (σ) are obtained from the minmax-delay parameters, as follows:

$$\mu = 0.5(d_{min} + d_{max})$$

$$\sigma = (d_{max} - d_{min})/6$$

The simulator computes logic values for signals using an event-driven procedure. In addition, a signal is also characterized by its *event-time distribution*. When an event (signal change) at an input of a gate causes a change at the output, the event-time distribution for the output is obtained as the *convolution* of the input event-time distribution and the gate-delay distribution of the gate [9]. The statistical-delay simulation in ATTSIM is referred to as the $K - \sigma$ delay simulation. The user can specify any value of K, which is used to multiply the standard deviations of all gates. In our analysis, we used $K = 6$.

INPUTS:

- Circuit netlist
- Vectors
- Delay option – *unit-delay, minmax, or K=?*
- Technology specification – e.g., 0.9μ CMOS

ALGORITHM:

1. Run zero-delay simulation and save results in database ZDT
2. Select a low clock frequency and run timing simulation, comparing primary output values with ZDT. If a mismatch occurs, lower the clock frequency until output agree with ZDT.
3. Reduce clock period in steps of 1 ns until a failure occurs.
4. Simulate repeatedly to determine the largest clock period with a 0.1 ns accuracy at which a failure occurs. This period corresponds to the GWF.
5. Postprocess the output waveform at the failing primary output for the vector-pair producing the error. Determine the period of GFF according to Fig. 5.

Figure 6: Algorithm for GFF and GWF determination

ATTSIM also takes common ambiguity into account by subtracting the "over pessimistic" contribution of signals originating at the same source. Common ambiguity cancellation is an important phase in predicting more realistic performance speeds. This is an improvement over alternative algorithms [11].

The overall procedure for determining GFF and GWF is given in Fig. 6. The circuit netlist is provided in EDIF. The timing accuracy (time-step for signal evaluation) of 0.1 ns was used. This is the default in ATTSIM and can be changed to be as small as 10^{-3} ns. The postprocessing required for GFF is accomplished by an output display and analysis tool (ODAN) provided by the simulator [2].

The procedure of Fig. 6 was implemented in a shell script to automatically execute the simulator and also to postprocess the results. A Perl program was used to generate the command files during the repeated executions of the simulator.

4 Experimental Results

Table 2 gives the results for several ISCAS'89 benchmark circuits. All circuits were operated in synchronous clocked sequential mode. Columns 2 and 3 show the number of vectors produced by Gentest [1, 3] and the stuck-at fault coverage. Untestable faults, if present, were counted as undetected. Thus, the actual fault efficiencies of these vectors are higher than the coverages shown.

The remaining columns give the values of GFF and GWF determined from unit-delay, minmax-delay and $6-\sigma$ statistical-delay simulations, respectively. Unit-delay frequencies are higher, but it represents a fictitious case. The other two delay models give lower test (GFF) and operating (GWF) frequencies, with $6-\sigma$ delay model being more pessimistic.

At the time this work was done, path delay tests were not available. We hope to analyze such vectors in the future. One would expect that delay tests will activate longer, ideally the longest, paths and will produce lower GFF and GWF.

5 Conclusion

GFF and GWF are important parameters in determining the circuit performance. For at-speed testing, one must determine the test clock rate. An ideal delay test for the critical (longest) path should only activate that path and should not activate any other shorter path. For such a test, the test frequency (GFF) and operating frequency (GWF) can be identical. When the test is not robust, it activates other shorter paths. This test can be robust for some shorter path. We then increase the test frequency (GFF) to actually measure the failure of that shorter path. In other words, the at-speed test should rely on testing only those paths that are robustly tested by the given vectors. If these paths are shorter than the critical paths, we must elevate the test frequency.

The $K-\sigma$ delay model leads to the most realistic performance values. GFF and GWF are, in general, functions of the given test vectors, the circuit topology, and the component delays. It is of utmost importance to have good set of test patterns before these frequencies could be reasonably sized. Good test patterns need to be able to exercise all critical paths in the circuit.

It should be pointed out that the GFF and GWF computed through our experiments only cover delay faults that follow the statistical distribution given by the cell library. The cell library delay values only reflect a *normal manufacturing process*. Obviously, catastrophic defects are not part of this assessment.

Table 2: GFF and GWF for ISCAS'89 benchmark circuits

Circuit	Number of vectors	Fault cov. %	Unit Delay		*Minmax* Delay		$6-\sigma$ Delay	
			GFF MHz	GWF MHz	GFF MHz	GWF MHz	GFF MHz	GWF MHz
S27	30	90.6	192	159	125	92	121	100
S344	144	93.1	116	68	81	55	74	56
S386	263	81.8	94	65	63	43	61	45
S641	467	84.8	86	61	72	49	67	52
S953	342	95.0	128	121	83	81	83	81
S5378	390	69.0	82	55	66	39	61	43

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