Finding Best Voltage and Frequency to Shorten Power-Constrained Test Time

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***Abstract*—In a digital test, supply voltage (V_{DD}), clock frequency (f_{test}), peak power (P_{MAX}) and test time (TT) are related parameters. For a given limit $P_{MAX} = P_{MAXfunc}$, normally set by functional specification, we find the optimum $V_{DD} = V_{DDopt}$ and $f_{test} = f_{opt}$ to minimize TT. A solution is derived analytically from the technology-dependent characterization of semiconductor devices. It is shown that at V_{DDopt} the peak power any test cycle consumes just equals $P_{MAXfunc}$ and f_{test} is fastest that the critical path at V_{DDopt} will allow. The paper demonstrates how test parameters can be obtained numerically from MATLAB, or experimentally by bench test equipment like National Instruments' ELVIS. This optimization can cut the test time of ISCAS'89 benchmarks in 180nm CMOS into half.**

***Keywords*-Reduced voltage test, Test time reduction, Scan test.**

I. Introduction

In the present day, complex integrated circuits are constructed using more than million gates. These devices comprise of many sequential elements such as memories and registers. The sequential circuits are tested using scan based test to check for defects that manifest as faults. However, owing to the size of the circuit, such tests can have many test cycles for a given set of test vectors and test frequency. Test frequency is determined by the length of the critical path and the maximum power allowed for the device. Often test power dissipation could be 3 to 4 times larger than the functional power dissipation [17]. Such high power dissipation can cause a good circuit to fail. Hence test cycles are run with significantly large periods when compared to the functional clock period. This increases test time and hence has an effect on the final chip cost [9].

Methods to reduce power dissipation can be broadly classified as test set dependent technique and test set independent technique. Adding to the length of test contributed by the size of the device, test set dependent methods that aim to reduce the power dissipation during tests in low power devices increases the test time further while trying to achieve high fault coverage using the low power vectors. Test set dependent techniques involve in exploiting the test patterns in such a way that the overall switching activity during test is lowered, thus reducing power. Techniques such as "don't care" fill or test pattern reordering are good examples of test set dependent techniques. In "don't care" fill technique the ATPG replaces the don't cares bits in the test pattern with 0 or 1 or just the adjacent bit value. This however would create large amount of test pattern to obtain high fault coverage due to the loss of randomization in the pattern after the fill. This in turn increase the test time while significantly reducing the power. In the test pattern reordering, the ATPG patterns are re-ordered in such a way that the Hamming distance between two vectors is minimized. This causes less transition in the circuit but increases the time to generate such tests. On the other hand, test set independent approach involves in implementing hardware modifications to reduce the power dissipation during scan test. Techniques like clock gating, inserting blocking gates that mask the non scan circuit during scan in and scan out are examples of test set independent approach. However these methods do not have any effect on the test time.

II. Prior Work

A recent approach to test time reduction for power constrained tests by Shanmugasundaram and Agrawal [20], [21] implements an activity monitor that monitors the activity in the scan chain of a built-in self-test (BIST) for a given test pattern set. The test clock frequency increases if the monitor observes a low switching activity in the scan chain or it decreases if the monitor observes high switching activity in the scan chain. The methodology attains 20-50% reduction in test time in BIST circuits with a little area overhead. Hashempour et al. [14] proposed a method that incorporates both ATE and BIST to minimize the overall test time. The BIST is used to identify all the easy to detect faults while the ATE is used later to find all the hard to detect faults. The reduction in test time is related to the effectiveness of the BIST to achieve high fault coverage such that the time spent by the ATE which might operate at a slower speed is minimum.

Reusable scan chains [16] and pattern overlapping [10] [11] eliminates unwanted scan chain operations by the use if patterns that resemble the previous pattern such that the number of scan shifting is minimum. Hence high reduction is achieved on availability of such patterns.

In this work we exploit the quadratic effect of supply voltage scaling on power and use it to reduce test time. Methods have been proposed [8] [15] to vary the power supply during normal operation to reduce power dissipation. Voltage reduction can also be beneficial in power constrained testing [12], [22], [23]. Power managed scan architecture proposed in [12] uses the on-chip dual voltage regulator to reduce the supply voltage during scan shift in order to decrease the power dissipated. However their methodology of dynamically reducing voltage,

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though reduces the total power, has an inverse effect on test time. In our method, instead of dynamically varying the power supply, we provide a quick and easy way to identify the supply voltage at which the test can run fastest. The optimum voltage is derived analytically as compared to an earlier Spice simulation based method [22]. Although, the present analysis requires technology characterization of formulas that is done with minimal amount of simulation. We show that it is possible to achieve significant reduction in test time during wafer sort without the need for additional hardware.

III. Analysis

In a power constrained test, the test clock period is limited by the maximum allowable power of the circuit. In general it can be related as

$$P_{MAXtest} = \frac{E_{MAXtest}}{T_{power}}$$

$$\Rightarrow T_{power} = \frac{E_{MAXtest}}{P_{MAXtest}} = \frac{C_L \times V_{DD}^2}{P_{MAXtest}}$$

where T_{power} is the test clock period at a given peak power limit $P_{MAXtest}$, $E_{MAXtest}$ is the maximum energy dissipated by any clock cycle during the entire test, and C_L is the total switched capacitance in clock cycle that consumes most energy due to rising signal transitions. Since the technique is implemented for stuck at fault test, the signal transitions in both scan shift and capture are accounted to find the cycle with maximum switching activity.

The maximum allowable power of the device is usually the maximum power dissipated during its functional operation for which the hardware is designed. Hence in a power constrained test, the maximum allowable power during test must not exceed the maximum power dissipated during functional operation, i.e. $P_{MAXtest} \leq P_{MAXfunc}$. The power constrained test clock period T_{power} is,

$$T_{power} \geq \frac{C_L \times V_{DD}^2}{P_{MAXfunc}} \quad (1)$$

The leakage power dissipation depends on the current flow in the circuit when it is in the steady state. Hence the power dissipation due to leakage will remain the same during test as during functional operation [13]. Although, in this paper we neglect the leakage power, which is a reasonable assumption for the 180nm technology used in the discussed examples, leakage power can be taken into account. Because our strategy is to lower the voltage and shrink the test clock period, the net effect will be to reduce the leakage power as well as leakage energy per cycle during test. In our analysis, the dynamic power which is a function of both signal transitions and short circuit power, is considered to dominate the total power dissipation.

One method to reduce the power dissipation in CMOS circuits is to reduce the supply voltage V_{DD}. However reducing supply voltage has an inverse relation with gate delay, i.e. the gate delay increases as the voltage is reduced. Sakurai and Newton [19] proposed a delay model that characterizes the delay based on the velocity saturation index α. An approximation of this model was stated in [18] called the alpha-power-law delay model and is re-written below

$$t_d \propto \frac{V_{DD}}{(V_{DD} - V_{TH})^{\alpha}}$$

where α is the velocity saturation index, V_{TH} is the threshold voltage of the device and V_{DD} is the supply voltage. This allows us to express the smallest structure constrained (or critical path constrained) test clock frequency as,

$$T_{critical} \geq K \times \frac{V_{DD}}{(V_{DD} - V_{TH})^{\alpha}} \quad (2)$$

where K is a proportionality constant, which depends upon the critical path structure, timing margin, etc..

To minimize the test time we find the smallest test clock period, T_{opt}, that will satisfy the power constraint (1) and critical path constraint (2). Thus, at any given voltage the optimum test period is given by

$$T_{opt} = \max\{\min T_{power}, \min T_{critical}\} \quad (3)$$

From equation (1) we observe that as the voltage is reduced T_{power} reduces. But from equation (2) $T_{critical}$ increases as the voltage is reduced. Thus if we plot equations (1) and (2) with respect to voltage, as the voltage reduces the two functions will cross each other at a point. The voltage V_{DDopt} at which the test time is minimum must satisfy:

$$T_{opt} = T_{power} = T_{critical} \quad (4)$$

This relation is evident in Figure 1 discussed in the next section. We make following assumptions in our analysis:

1. Variation in threshold voltage V_{TH} due to changes in supply voltage is not drastic and V_{TH} is assumed to be constant for the supply voltage interval of interest.

2. Critical path remains unchanged as supply voltage changes. Thus, the value of K is assumed to be independent of the supply voltage.

We equate the right hand sides of (1) and (2) according to (4) and substitute $V_{DD} = V_{DDopt}$:

$$T_{opt} = \frac{C_L \times V_{DDopt}^2}{P_{MAXfunc}} = \frac{K \times V_{DDopt}}{(V_{DDopt} - V_{TH})^{\alpha}} \quad (5)$$

We make two useful observations about the test conducted at supply voltage V_{DDopt} that satisfies (5):

- For shortest test time, the test clock period T_{opt} is the minimum allowed by the critical path delay at V_{DDopt}.
- The maximum power for a test cycle, $C_L \times V_{DDopt}/T_{opt}$, equals the peak power specification $P_{MAXfunc}$.

These observations help us experimentally find the optimum test time parameters in Section V. To analytically obtain V_{DDopt} we derive a polynomial equation:

$$V_{DDopt}^{\frac{1}{\alpha}+1} - V_{TH} \cdot V_{DDopt}^{\frac{1}{\alpha}} - (\frac{K \times P_{MAXfunc}}{C_L})^{\frac{1}{\alpha}} = 0 \quad (6)$$

or

$$V_x^{\alpha+1} - V_{TH} \cdot V_x - \gamma = 0 \quad (7)$$

where $V_x = V_{DDopt}^{\frac{1}{\alpha}}$ and $\gamma = (\frac{K \times P_{MAXfunc}}{C_L})^{\frac{1}{\alpha}}$

Since $\alpha = 1$ if the device is completely velocity saturated and $\alpha = 2$ is the device has no velocity saturation [18] [19], equation (7) is a polynomial of degree three or lower, which is solvable. Knowing the voltage V_{DDopt} for the shortest test time, the corresponding shortest test clock period can be obtained from (5) as,

$$T_{opt} = \frac{C_L \times V_{DDopt}^2}{P_{MAXfunc}} \quad (8)$$

The optimum test frequency is then

$$f_{opt} = \frac{1}{T_{opt}}$$

Here f_{opt} is the maximum power constrained test frequency.

We used MATLAB to obtain the roots of the polynomial equation (7). The values for K, α, $P_{MAXfunc}$ and effective maximum switched load capacitance C_L during any test cycle can be obtained through simulation at nominal voltage.

IV. Solving for V_{DDopt}, f_{opt} and TT_{opt}

In this section we demonstrate with an example how to obtain the optimum voltage V_{DDopt}, optimum frequency f_{opt}, and the total test time TT_{opt}. The optimum voltage will be the minimum voltage at which the test can run fastest without exceeding the maximum power limit of the device and without being structurally constrained due to increase in critical path delay because of scaling the supply voltage.

As an example, we use s298 ISCCAS'89 sequential benchmark circuit synthesized for scan test in TSMC 180nm technology using Mentor Graphics' Leonardo Spectrum tool [5]. The nominal voltage for this technology is 1.8V and the threshold voltage is 0.39V. The critical path delay obtained through static timing analysis (STA) using Leonardo Spectrum [5] was 1.5ns or 666MHz. To find V_{DDopt} using equation (7) we need values for the proportionality constant K, maximum allowable power limit $P_{MAXfunc}$ and the maximum switched capacitance C_L, that will determine γ.

The alpha power law model given in equation (2) is an approximate method to find the critical path delay for any circuit for a given supply voltage and threshold voltage. The value for α, the velocity saturation index, in equation (2) ranges between 1 and 2 [18] [19] and can be found using methods described in [7] and [19]. It can also be obtained from a simple curve fitting to delay values at different voltages for a chain of inverters. In our experiment for 180nm technology the value for α was found to be 2 using the latter method.

We can now rewrite equation (2) to find the value for K as follows:

$$K = T_{critical} \times \frac{(V_{DD} - V_{TH})^{\alpha}}{V_{DD}}$$

To trigger the critical path for observe the delay we obtained a path delay vector set using Mentor Graphics' Fastscan [4]. However, the 7-gate critical path reported by STA was found to be a false path and hence we chose the next longest path containing 6 of the 7 gates in the critical path. The STA for this path was given as 0.77ns. Post synthesis timing simulation of the CUT using Mentor Graphics Modelsim with a period of 0.77ns was found to pass the test. The value for the proportionality constant K for this path was calculated to be 0.85. Value of K depends on the critical path of the circuit, hence based on assumption 2 in Section III the value is kept constant.

The maximum allowable power limit for a circuit is normally given as a specification in the datasheet. In a power constrained test the power dissipated during test must be kept under that limit. In the absence of a known power limit for our CUT, we determined the maximum allowable power by simulating 100 random vector patterns in functional mode and measured the power dissipated per cycle using Synopsys Nanosim transistor level simulator at the nominal voltage of 1.8V and a frequency of 500MHz. The maximum power over the entire functional operation is assumed to be the upper bound for the power during test. For the CUT in this example the upper bound is measured as 1.2mW.

The next unknown is the maximum switched capacitance C_L. It is defined as the effective switched load capacitance of the circuit during maximum rising signal transitions caused by any test cycle. Energy consumed during that cycle is,

$$E_{MAXtest} = C_L \times V_{DD}^2$$

where C_L = maximum switched capacitance of the test pattern that causes the most rising signal transitions. Therefore,

$$C_L = \frac{E_{MAXtest}}{V_{DD}^2}$$

The value of $E_{MAXtest}$ can be obtained by simulating the test patterns at any arbitrary (slow) frequency f and measuring the maximum power $P_{MAXtest}$ for a clock cycle, i.e.,

$$E_{MAXtest} = \frac{P_{MAXtest}}{f}$$

where f is any frequency slower than the maximum allowed by the critical path.

Once the value for $E_{MAXtest}$ is obtained, C_L can be obtained from the equation above. For the CUT in this example the value for C_L is obtained as 2.04pF. Table I summarizes the values obtained above. Substituting these values into the expression for γ following equation (7) we get $\gamma = 0.7158$ and equation (7) becomes,

TABLE I
PARAMETER VALUES FOR S298 BENCHMARK SYNTHESIZED IN 180NM CMOS TECHNOLOGY ($V_{DD} = 1.8$V, $V_{TH} = 0.39$V).

Parameter	Value
$P_{MAX(func)}$	0.0012W
C_L	2.04pF
K	0.85
α	2

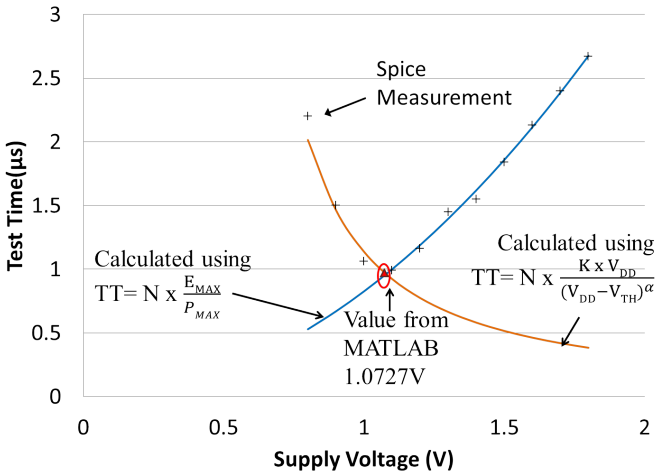

Fig. 1. Simulated and calculated curves using test period and functional period at various voltages. The direct approach using MATLAB (circled) matches the cross point of the curves obtained analytically using the periods calculated from equations (1) and (2) and the results obtained from Hspice ("plus" data points) in [22].

$$V_X^3 - 0.39V_X - 0.7158 = 0$$

We use a numerical solver in MATLAB to find the roots for V_X. We obtain 3 roots, two complex and one real. Since the supply voltage is a real number, it is logical to consider only the real root and discard the two complex roots. Solving for V_{DDopt} from V_X we get $V_{DDopt} = 1.0727$V. This is the optimum voltage at which the test can run fastest. Since at this voltage the test is still power constrained we can calculate T_{opt} from equation (1) where $T_{test} = T_{opt}$ which gives us $T_{opt} = 1.95ns \Rightarrow f_{opt} \approx 511$MHz.

The total test time for the CUT can be calculated as

$$TT_{opt} = N \times T_{opt}$$

where N is the total number of test cycles. For the CUT in this example $N = 498$ hence the total test time is $TT_{opt} = 0.971\mu$s.

Figure 1 shows the calculated test time plots using equations 1 and 2, at various voltages for s298 benchmark circuit. The circled data point indicate the optimum voltage value obtained from the numerical analysis. The values measured from Hspice at various voltages in [22] are shown in the curve "Spice Measurement". It is readily observed from the graph that the numerical analysis to obtain the optimum voltage is in accordance with the Hspice measurement.

The procedure described in this section is repeated for several ISCAS'89 benchmark and the results are tabulated in Table II. Table III gives the results from [22] based on Nanosim Spice [3] simulation. It is noted that the values obtained from the numerical analysis are very close to the values measured through Hspice simulation. Unlike [22] where the optimum voltage is obtained through simulations for closely spaced voltages to find the point before the circuit become structure constrained, to solve the polynomial equation (7) for a given $P_{MAXfunc}$, we need to simulate the circuit only once at the nominal voltage to find the constants. For instance if the optimum voltage using Hspice simulations is achieved after 10 simulations, the time taken to obtain the optimum supply voltage and test time using the numerical analysis, is reduced by $\frac{1}{10}$. In Table II it was observed that if the value for the chosen $P_{MAX(func)}$ is closer to the power dissipated during test, then the reduction obtained in test time using reduced voltage is not much. This is because, when the power dissipated by the test is closer to the rated power, the test runs at a speed closer to the functional speed and any reduction in supply voltage make the test structure constrained. This is seen in circuits s1423 and s15850. On the other if the power dissipated during test is significantly greater than the rated power then significant reduction in test time is observed as in s298 and s382. Most circuits today have the test power $2\times$ to $4\times$ the functional power [17], hence significant reduction in test time is attainable.

V. PEAK POWER AND CRITICAL PATH FREQUENCY MEASUREMENTS

A. Hardware Setup

National Instruments ELectronic Virtual Instrumentation Suite II+ (NI ELVIS) [2] serves equally well as a bench-top test equipment and prototyping board. We used NI ELVIS to measure peak power per cycle and the maximum circuit test frequency for a given supply voltage. The circuit used for measurements was the Altera DE2 Field Programmable Gate Array (FPGA) board [6]. DE2 board houses Altera Cyclone-II 2C35 FPGA. Benchmark circuit S298 was programmed on this FPGA. Figure 2 shows the test setup for the power and maximum test frequency measurements. The DE2 board is powered through the variable power supply available on NI ELVIS. S298 circuit input and output, including scan-in, and scan enable are configured to the external pins of the DE2 board. These pins are in turn connected to the programmable digital Input/Output (IO) pins available on NI ELVIS. Test program is written in LabVIEW [1] on a PC, and the test patterns are sent to NI ELVIS through a Universal Serial Bus (USB) connection. Stored test patterns are then applied to the circuit under test (in our case the DE2 board) from NI ELVIS, and the response is captured and compared for every test vector.

B. Peak Power and Frequency Measurements

Figure 3 shows the peak power per cycle and maximum test frequency plotted as a function of the supply voltage. As the DE2 board comprises of number of peripherals like the seven-segment display, several LED, several different IO drivers, etc., the absolute power numbers measured from the

TABLE II
ANALYTICALLY OBTAINED V_{DDopt} AND f_{opt} FOR MINIMUM SCAN TEST TIME OF ISCAS'89 CIRCUITS IN 180NM CMOS ($\alpha = 2$, $V_{TH} = 0.39$V).

Circuit name	Proportionality constant K ($\times 10^{-9}$)	Maximum switched capacitance C_L (pF)	Total scan test cycles N	Peak per cycle power $P_{MAXfunc}$ (W)	Nominal voltage (1.8V) test		Optimum voltage test			Test time reduction (%)
					Test clock frequency (MHz)	Test time (μs)	Supply V_{DDopt} (Volts)	Test freq. f_{opt} (MHz)	Test time (μs)	
s298	0.85	2.04	498	0.0012	187	2.66	1.07	511	0.97	63
s382	1.28	3.07	704	0.0029	300	2.35	1.34	532	1.32	44
s713	3.31	6.23	809	0.0027	136	5.89	1.41	223	3.62	38
s1423	6.63	9.78	4649	0.0045	141	33.00	1.72	155	29.89	12
s13207	4.50	60.3	41266	0.0213	110	378.00	1.44	170	242.00	36
s15850	5.79	362	67624	0.1781	151	445.58	1.70	172	392.00	12
s38417	4.97	187	181536	0.0737	121.8	1491.90	1.52	169	1100.00	26
s38584	4.42	263	186159	0.1106	129	1437.09	1.50	186	1000.50	30

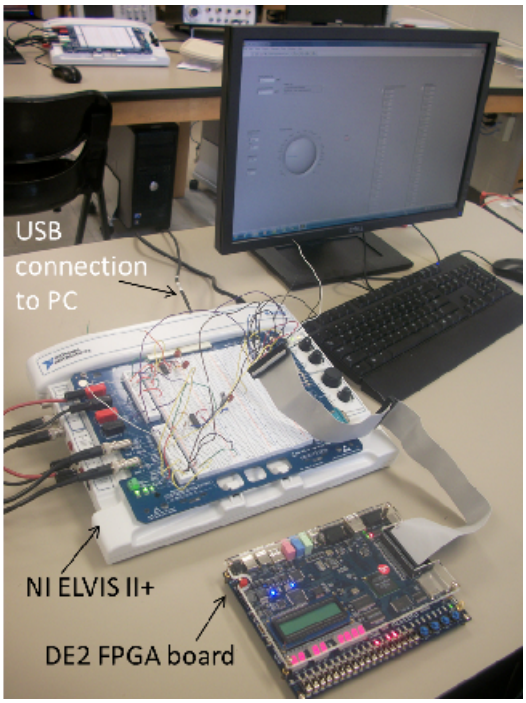

Fig. 2. Test setup for measuring peak power per cycle and maximum test frequency for an Altera DE2 FPGA board (with all its peripherals) using the NI ELVIS II+ bench-top prototyping board.

supply voltage and current product will be dominated by these peripheral components rather than the actual circuitry on the FPGA. We, therefore, corrected the measured supply-power by removing the steady state power component in each cycle. The remaining power component, which is the switching (or dynamic) power, is presumably dominated by CMOS circuitry on the FPGA. The dynamic power curve is shown in blue with circular markers at the measured voltage points on the graph in Figure 3. We found that the peak dynamic power per cycle increases as a square of the supply voltage in the range of 1.8V–5.4V, well in agreement with theory. For supply voltages below 1.8V, even very low test frequencies result in erroneous results, which is plausible since the nominal voltage specified for the board is 3.3V, and one or more of the IO drivers may not be operational at voltages below 1.8V. Even though the commonly used nominal supply voltage for CMOS logic

TABLE III
OPTIMUM TEST CONDITIONS FROM DETAILED HSPICE SIMULATION [22].

Circuit	Peak per cycle Power (W) $P_{MAXfunc}$	V_{DDopt} (V)	Test clock frequency (MHz) f_{opt}	Test time reduction (%)
s298	0.0012	1.08	500	62.5
s382	0.0029	1.35	521	42.5
s713	0.0027	1.45	227	40.0
s1423	0.0045	1.70	158	11.0
s13207	0.0213	1.45	165	40.3
s15850	0.1781	1.65	170	10.7
s38417	0.0737	1.50	175	30.5
s38584	0.1106	1.50	187	31.0

circuits at the 90nm technology node is about 1.2V, we could only control the supply to the DE2 FPGA board in the range 1.8V to 5.4V. Because the tests destined for s298 implemented on the FPGA chip were applied through edge connectors and other logic on the board, the whole process ran essentially like a board test rather than a chip test.

The maximum test frequency, in practice, is limited by the structural critical path delay of the circuit; however, in the current setup, it is limited by the speed of the IO drivers on the FPGA board and the maximum allowable sampling frequency of NI ELVIS. The maximum test frequency at each supply voltage also corresponds to frequency at which maximum power per cycle is dissipated. This curve is shown in green with diamond markers at the measured voltage points in Figure 3. The maximum operating frequency at each supply voltage step was found by starting at an initial frequency and increasing it until the point where the circuit output no longer matches the ideal output. The highest frequency at which the circuit output matches the ideal output is taken as the peak operating frequency.

C. Minimizing Test Time for Given Peak Power Limit

For a circuit under test with a given peak power limit, $P_{MAXfunc}$, the experimental data of Figure 3 readily gives both the supply voltage V_{DDopt} and test frequency f_{opt} that minimize the test time of the power constrained test. This is done by using the two observations made following equation (5). For example, suppose we have a peak power limit

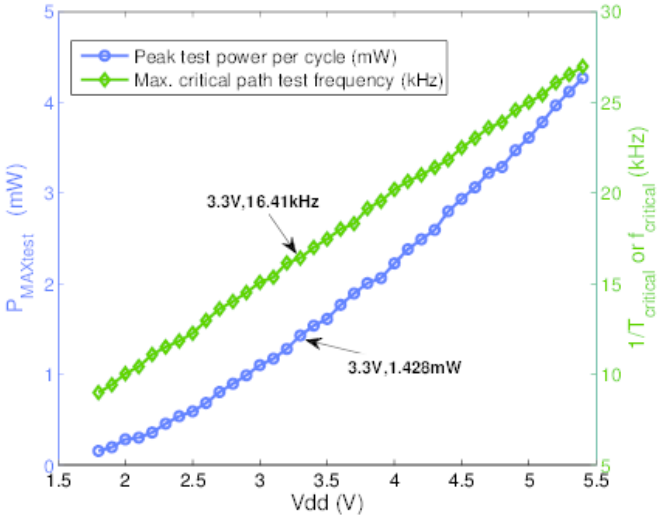

Fig. 3. Measured values of maximum power consumed per cycle (in blue) and maximum test frequency (in green) plotted as a function of the supply voltage for the Altera DE2 FPGA board tested using NI ELVIS II+ bench-top prototyping board. Switching power is dominated by the CMOS circuitry contained on the board. The FPGA itself is programmed with the function of s298 benchmark with scan.

$P_{MAXfunc} = 0.5$mW. At the nominal supply voltage of 3.3V, the test power dissipation is 1.428mW and maximum structural clock frequency is 16.4 kHz. To keep the test power under 0.5mW, the test must be run at $16.4 \times 0.5/1.428 = 5.74$kHz. From Figure 3, for $P_{MAXtest} = P_{MAXfunc} = 0.5$mW, we should lower V_{DD} to $V_{DDopt} = 2.5$V, which gives a test frequency of $f_{opt} = 12.5$kHz. Thus, test time will be reduced by a factor $5.74/12.5 = 0.46$.

Such low clock frequencies are typical of printed circuit boards. We are in the process of testing chips directly on a high speed tester.

VI. Conclusion

In this work we have given an analytical procedure to identify the supply voltage and clock frequency at which the power constrained test time is minimized. A numerical solution gives close enough values as obtained from detailed Hspice simulation. The methodology also allowed experimental determination of the test conditions for a logic board system using the NI ELVIS bench test equipment, demonstrating the feasibility of such an application. The implementation of similar experiments for chip test is in progress on Advantest T2000GS Automatic Test Equipment (ATE). Recent work shows that further reduction in test time is possible if an asynchronous test clock is used besides a properly selected voltage [23].

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