

# Bounds on Defect Level and Fault Coverage in Linear Analog Circuit Testing

*Area E - System Integration and Test, and VLSI Chip Design and Test*

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## Abstract

*Transfer function coefficients (TFC) are widely used to test linear analog circuits for parametric and catastrophic faults. This paper presents closed form expressions for an upper bound on the defect level (DL) and a lower bound on fault coverage (FC) achievable in TFC based test method. The computed bounds have been tested and validated on several benchmark circuits. Further, application of these bounds to scalable RC ladder networks reveal a number of interesting characteristics. The approach adopted here is general and can be extended to find bounds of DL and FC of other parametric test methods for linear and non-linear circuits.*

## Index Terms

*Analog circuit testing, Catastrophic faults, Defect level, Fault coverage, Parametric faults, Transfer function*

## I. INTRODUCTION

Faults in analog circuits can be fundamentally divided into two categories, namely, catastrophic and parametric[1]. Catastrophic faults are those in which the circuit component concerned displays extreme deviant behaviour from its nominal value. For example, in a resistor such a fault could either be an electrical -open or -short. Such faults are easy to uncover, as they manifest themselves as a sizable deviation in circuit output or performance. On the other hand, parametric faults are fractional deviations in circuit components from their nominal values. They manifest themselves as subtle deviations in output or performance of the circuit. It is therefore a non-trivial problem to uncover parametric faults. Further, among the analog test methods available it is a significant problem to characterize “how good” such methods are to uncover parametric faults, in terms of defect level (DL) and fault coverage (FC) that are achievable. In this work an important step is taken in that direction by finding bounds (or limits) of achievable DL and FC in testing linear analog circuits.

Parametric testing of analog circuits has been discussed at length in literature [2], [3], [4], [5], [6], [7]. A popular and elegant method was proposed by Savir and Guo [8], in which, analog circuit under test is treated as a linear time invariant (LTI) system. The transfer function (TF) of this LTI system is computed based on the circuit netlist. Note that the coefficients in the numerator and denominator of the transfer function (TF), herein referred to as Transfer Function Coefficients (TFC), are functions of circuit parameters. It now follows that any drift in circuit parameters from their fault free (nominal) values will also result in drifts of the coefficients, as they are linear functions of circuit parameters. As a result min-max bounds for the coefficients of a healthy circuit are found and these are used to classify the CUT as good or faulty. Reference [4] shows some limitations in parametric analog testing by treating CUT this way. However, there has been no effort to quantify the achievable FC and DL in TFC based testing of analog circuits. In this work we have derived closed form expressions for upper bound on DL and lower bound on FC.

The approach used in [8] is to find the parametric faults by measuring the TFC estimates of the CUT. Minimum size detectable fault (MSDF) in this method is defined as the minimum fault size or minimum fractional drift of the circuit parameter that will cause the circuit characteristic (in this case the TFC) to lie beyond its permissible limits [8]. In general, computation of MSDF for a circuit parameter is a non-linear optimization problem and is computationally expensive to evaluate MSDF of all the circuit parameters. However we have some respite in TFCs of linear analog circuit being linear functions of the circuit parameters. This implies that TFCs of the circuit take min-max values when at least one of the circuit parameter is at the edge of its tolerance band (fault free drift range) [8]. This fact is used to avoid solving the non-linear optimization problem. Instead, the circuit is simulated for all combinations of extreme values taken by circuit parameters in its fault free drift range. The minimum deviation in circuit parameters causing the coefficients to move out of their min-max bands is thus obtained and is called nearly minimum size detectable fault (NMSDF). The price paid in the process is the non-zero difference between NMSDF and MSDF. In the paper we quantify this difference and thereby derive bounds for DL and FC achievable through TFC based testing methods. Further, we also present a tradeoff between computational overheads of simulation vis-à-vis the effort required to solve the non-linear optimization problem based on the DL desired.

This paper is organized as follows. In Section 2 we formulate the problem. Section 3 describes our approach and present analytical proofs for the bounds on DL and FC. Section 4 comprises the simulation results for some well-known circuits. Section 5 is a discussion on “simulation–optimization” tradeoff based on bounds of DL and FC. Section 6 concludes the paper.

## II. PROBLEM FORMULATION

A linear analog circuit [9], [10], [11] can be represented as a LTI system whose transfer function is given by

$$H(s) = K \frac{s^\lambda + \sum_{k=0}^{\lambda-1} a_k s^k}{s^\mu + \sum_{k=0}^{\mu-1} b_k s^k} \quad (\lambda < \mu) \quad (1)$$

Consider a linear analog circuit made up of  $N$  circuit components (alternatively called circuit parameters), each of them having a nominal value of  $p_{ni} \forall i = 1 \dots N$ . Let the fault free drift range of each component be  $\alpha$  about its nominal value.

Let the set  $\psi$  be defined as

$$\psi = (\chi, u_0, \dots, u_\lambda, v_0, \dots, v_\mu) \quad (2)$$

such that

$$\begin{aligned} \chi &\in K_H, u_0 \in A_0, u_1 \in A_1, \dots, u_\lambda \in A_\lambda \\ v_0 &\in B_0, v_1 \in B_1, \dots, v_\mu \in B_\mu \end{aligned}$$

for all

$$p_{ni}(1-\alpha) \leq p_i \leq p_{ni}(1+\alpha) \quad \forall i = 1 \dots N$$

The set of all fault free or undetectable fault values taken by any coefficient  $a_i$  in (1) is contained in set  $A_i$ . That is  $A_i$  consists of all values in the closed interval  $A_i = [a_{i,min}, a_{i,max}]$ . Thus  $\psi$  as defined in (2) comprises of all combinations of coefficients of “good” circuit [8]. Let  $C_k$  be one of the coefficients of the LTI system transfer function in (1). Clearly  $C_k$  is a function of at least one or more circuit parameters  $p_i \forall i = 1 \dots N$ . Each of the coefficients,  $C_k \forall k = 0, \dots, (\lambda + \mu + 1)$  is enclosed in an  $N$ -dimensional hypercube spanned by the circuit parameters. The volume of this hypercube depends on the fault free drift range of the circuit parameters that determine  $C_k$ . As the extremities of any coefficient  $C_k$  of the transfer function occur when at least one or more of its parameters are at the edges of its fault free range, the circuit is simulated only at the boundary hyper planes enclosing the hypercube. The maximum and minimum values of the coefficient obtained along these vertices is concluded as the maximum and minimum bounds of the coefficient  $C_k$ .

We formally define some of the terms as they are used in this paper.

*Definition 1:* Minimum size detectable fault (MSDF)  $\rho_i$  of a parameter  $p_i$  is defined as the fractional change in its value to push the circuit to faulty - fault free interface with all the other parameters remaining at their nominal values.

*Definition 2:* Nearly minimum size detectable fault (NMSDF)  $\rho_i^*$  of a parameter  $p_i$  is defined as the fractional change in its value to push the circuit to its faulty region with all the other parameters being at their nominal values. Note that  $\rho_i^* \geq \rho_i \forall i = 1 \dots N$ .

*Definition 3:* Coefficient of uncertainty ( $\epsilon_i$ ) is defined as the assumed difference between the NMSDF and MSDF for the  $i^{th}$  circuit parameter. That is,

$$\epsilon_i = \rho_i^* - \rho_i \quad (3)$$

*Definition 4:* Defect level (DL) of a test procedure is defined as the probability of a faulty circuit passing the test as a fault free circuit.

*Definition 5:* Fault coverage (FC) of a test procedure is defined as the fraction of all detectable faults that can be uncovered by the test procedure on the CUT.

Consider a TFC  $C_k$  being a function of parameters  $p_1$  and  $p_2$ . The hypercube enclosing  $C_k$  is shown in Figure 1. MSDF value of  $p_1$  and  $p_2$  is found by solving a non-linear optimization problem. The objective of the problem being to maximize (or minimize)  $C_k$  with constraint on  $p_1$  and  $p_2$  allowing a drift of  $\pm\alpha$  about its nominal value. An example of MSDF calculation has been illustrated in [3]. NMSDF of  $p_1$  and  $p_2$  is obtained by simulating the circuit at the vertices of the hypercube and measuring the fractional change in the value of  $C_k$ . In general the MSDF ( $\rho$ ) and NMSDF ( $\rho^*$ ) values of parameters for drifts above and below its nominal values are not the same. However for the sake of developing a conservative bound and ease of calculation we consider  $\rho = \text{Min}(\rho_\uparrow, \rho_\downarrow)$  and  $\rho^* = \text{Max}(\rho_\uparrow^*, \rho_\downarrow^*)$ . Where  $\rho_\uparrow$  and  $\rho_\downarrow$  denote positive and negative MSDF and  $\rho_\uparrow^*$  and  $\rho_\downarrow^*$  denote positive and negative NMSDF.

Shaded region  $\Lambda$  in Figure 1 shows the region of uncertainty and any parameter drift leading to coefficient lying in this region goes undetected. It is this region that contributes to the DL incurred by observing coefficient  $C_k$  denoted as  $DL_{C_k}$ .

### III. OUR APPROACH

#### A. Bounding Defect level

The values taken by circuit parameters can be modeled as independent and identically distributed random variables whose mean is the nominal fault-free value and standard deviation ( $\sigma$ ) is the tolerance value of circuit parameter [12].

1) *Two parameter case:* Here we assume a normal distribution of the parameters  $p_1$  and  $p_2$  with mean same as their nominal values ( $p_{1n}$  and  $p_{2n}$ ) and variance  $\sigma^2$ . The DL incurred due to coefficient  $C_k$  alone is obtained by integrating the joint probability density function of parameters  $p_1$  and  $p_2$  over the shaded area  $\Lambda_k$  shown in Figure 1 and is given by (4).

$$DL_{C_k} = \int_{\Lambda_k} f_{p_1, p_2}(x, y) dx dy \quad (4)$$

$f_{p_1, p_2}(x, y)$  in (4) is the joint p.d.f of  $p_1$  and  $p_2$  and is given by (5).

$$f_{p_1, p_2}(x, y) = \frac{1}{2\pi\sigma^2} \exp\left(\frac{-(x - p_{1n})^2}{2\sigma^2} + \frac{-(y - p_{2n})^2}{2\sigma^2}\right) \quad (5)$$

We define  $Q(x)$  in (6) below as the integral over the limits  $[x, \infty)$  of zero mean and unit variance normal distribution [13].  $S_1$  and  $S_2$  are defined in (7) and (8), respectively.

$$Q(x) = \frac{1}{\sqrt{2\pi}} \int_x^{\infty} \exp\left(\frac{-u^2}{2}\right) du \quad (6)$$

$$S_1 = \int_{p_{1n}(1-\alpha)}^{p_{1n}(1+\alpha)} \int_{p_{2n}(1-\alpha)}^{p_{2n}(1+\alpha)} f_{p_1, p_2}(x, y) dx dy \quad (7)$$

$$S_2 = \int_{p_{1n}(1-\alpha)}^{p_{1n}(1+\alpha)} \int_{p_{2n}(1-\alpha+\epsilon)}^{p_{2n}(1+\alpha-\epsilon)} f_{p_1, p_2}(x, y) dx dy \quad (8)$$

$S_1$  and  $S_2$  evaluate to the following  $Q$  functions on integrating over the areas shown in Fig.1. The DL obtained on observing only a single coefficient  $C_k$  is given by (9).

$$S_1 = \left\{ Q\left(\frac{-\alpha}{\sigma}\right) - Q\left(\frac{\alpha}{\sigma}\right) \right\}^2$$

$$S_2 = \left\{ Q\left(\frac{-\alpha}{\sigma}\right) - Q\left(\frac{\alpha}{\sigma}\right) \right\} \left\{ Q\left(\frac{-\alpha + \epsilon}{\sigma}\right) - Q\left(\frac{\alpha - \epsilon}{\sigma}\right) \right\}$$

$$DL_{C_k} = S_1 - S_2 \quad (9)$$

2) *Generalizing the bound:* The result in (9) can be extended to case where coefficient  $C_k$  depends on all of the  $N$  circuit parameters. Note that to get an upper bound in this case we take only one parameter to be at its fault free edge while other parameters can be anywhere in the fault free band of their values [8]. The maximum DL in this case due to observing  $C_k$  alone is given by (10)

$$DL_{C_k} = \int_{\Lambda_k} \cdots \int f_{p_1, p_2, \dots, p_N}(x_1, x_2, \dots, x_N) dx_1 \cdots dx_N \quad (10)$$

*Theorem 1.* For TFCs that are functions of the same circuit parameters, a parametric fault ( $\rho_n$ ) for any  $n = 1 \dots N$ , such that  $\rho_n \geq \rho$  can escape being detected if and only if it induces all the TFCs into their regions of uncertainty.

*Proof:* By definition, an undetectable fault leads to combinations of TFCs which belong to set  $\psi$ , as defined in (1). Any combination of TFCs not belonging to set  $\psi$  is a fault. Such a fault is detectable if at least one of the TFCs is beyond its min-max bound, which is obtained on substituting the NMSDF values of circuit parameters it depends on. This implies a fault can be undetectable only if it induces none of the TFCs beyond its min-max value. That is to say all coefficients are in their regions of uncertainty.

*Corollary 1:* If  $\kappa_i$  were the event that the  $i^{th}$  coefficient is in its region of uncertainty, then the event  $\kappa$  of all coefficients being in their regions of uncertainty is given by

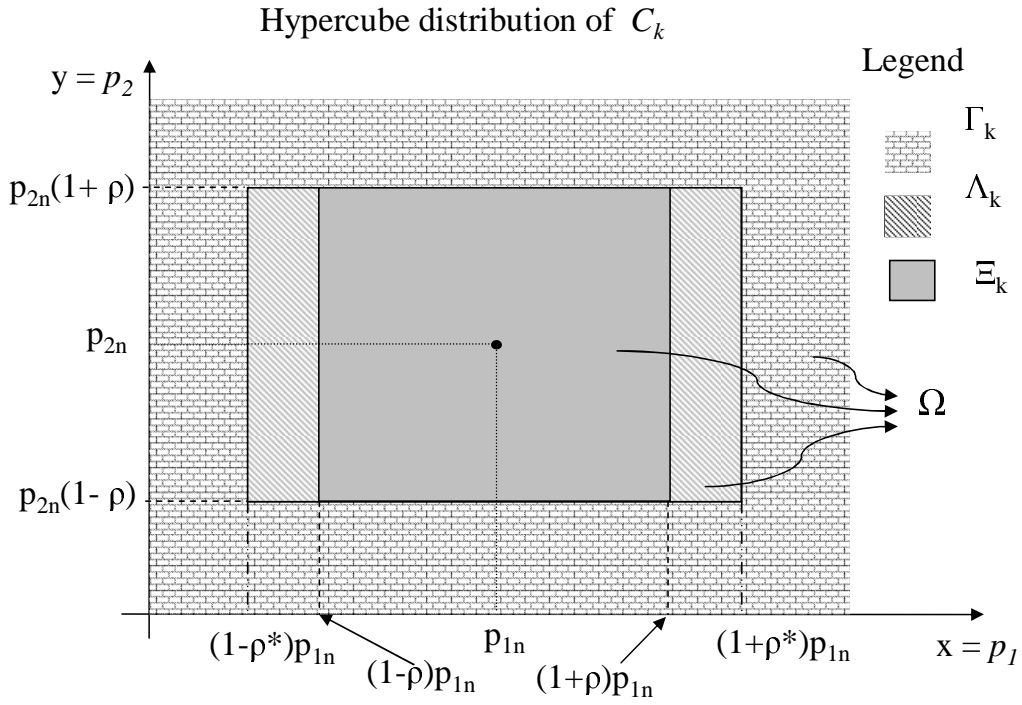


Fig. 1. Hypercube around coefficient  $C_k$  and associated regions.

$$\kappa = \prod_{i=0}^{\lambda+\mu+1} \kappa_i \quad (11)$$

$$\wp(\kappa) = \wp\left(\prod_{i=1}^{\lambda+\mu+1} \kappa_i\right) \quad (12)$$

$$\Rightarrow \wp(\kappa) \leq \wp(\kappa_i)$$

Where  $\wp(\kappa)$  denotes probability of event  $\kappa$ . Equation (12) follows from the fact that  $\kappa_i \supseteq \kappa$ . We have (13) from (12) and the definition of DL as stated in definition 4.

$$DL_{C_k} \geq DL \quad (13)$$

From (10) the upper bound on  $DL_{C_k}$  and DL is given by (14) for N circuit parameters and coefficient of uncertainty in each parameter being same and equal to  $\epsilon$ .

$$DL \leq DL_{C_k} \leq \left\{ Q\left(\frac{-\alpha}{\sigma}\right) - Q\left(\frac{\alpha}{\sigma}\right) \right\}^N - \left\{ Q\left(\frac{-\alpha}{\sigma}\right) - Q\left(\frac{\alpha}{\sigma}\right) \right\} \left\{ Q\left(\frac{-\alpha+\epsilon}{\sigma}\right) - Q\left(\frac{\alpha-\epsilon}{\sigma}\right) \right\}^{N-1} \quad (14)$$

An analog circuit is typically designed anticipating  $\pm\sigma$  variation in its component values [12], where  $\sigma$  is the standard deviation or tolerance of a parameter about its nominal value and is usually known a priori as a specification of the device. We can therefore assume fault free drifts of  $\pm\alpha$  about the nominal value of the circuit parameter to be equal to  $\pm\sigma$  variation in the value of parameter. Substituting  $\pm\alpha = \pm\sigma$  in the equation (14), we get a conservative bound on DL and is given by (15).

$$DL \leq 0.8427^N - 0.8427 \left\{ Q\left(-1 + \frac{\epsilon}{\sigma}\right) - Q\left(1 + \frac{-\epsilon}{\sigma}\right) \right\}^{N-1} \quad (15)$$

### B. Bounding Fault Coverage

Just as we dealt with the problem of bounding the DL, we shall first consider the two parameter case and then generalize this result to N parameters.

1) *Two parameter case:* Here we assume a normal distribution of the parameters  $p_1$  and  $p_2$  with mean same as their nominal values ( $p_{1n}$  and  $p_{2n}$ ), variance  $\sigma^2$  and their probability distributions being independent of each other. The FC achievable by observing coefficient  $C_k$  alone is obtained by integrating the joint probability density function of parameters  $p_1$  and  $p_2$  over the shaded area  $\Gamma_k$  shown in Fig. 1 and is given by (16).

$$FC_{C_k} = \int_{\Gamma_k} f_{p_1, p_2}(x, y) dx dy \quad (16)$$

Region  $\Gamma_k$ , given by (17), is the complement of union of region of uncertainty  $\Lambda_k$  and fault free space  $\Xi_k$  of coefficient  $C_k$  in I quadrant, where  $p_1, p_2 \in (0, \infty)$  which is the entire region in the I quadrant denoted as  $\Omega$ .

$$\Gamma_k = \Omega \setminus (\Lambda_k \cup \Xi_k) \quad (17)$$

$$S_{\Omega} = \left\{ Q\left(\frac{-p_{1n}}{\sigma}\right) Q\left(\frac{-p_{2n}}{\sigma}\right) \right\} \quad (18)$$

$S_{\Omega}$  in (18) gives probability of the region under  $\Omega$ . From (17) and (18), we have  $FC_{C_k}$  given by (19).

$$FC_{C_k} = \left\{ Q\left(\frac{-p_{1n}}{\sigma}\right) Q\left(\frac{-p_{2n}}{\sigma}\right) \right\} - \left\{ Q\left(\frac{-\alpha}{\sigma}\right) - Q\left(\frac{\alpha}{\sigma}\right) \right\}^2 \quad (19)$$

In general, nominal value of parameter is much greater than its tolerance [12]. We can therefore fairly assume  $p_{in} = 5\sigma \forall i = 1 \dots N$  and  $\pm\alpha = \pm 3\sigma$  in (19) to find  $FC_{C_k}$  for two parameters.

2) *Generalizing the bound:* Equation (16) can be extended to N parameters as in (20).

$$FC_{C_k} = \int_{\Gamma_k} \dots \int f_{p_1, p_2, \dots, p_N}(x_1, x_2, \dots, x_N) dx_1 \dots dx_N \quad (20)$$

*Theorem 2.* For TFCs that are functions of the same circuit parameters, a parametric fault ( $\rho_n$ ) for any  $n=1 \dots N$  such that  $\rho_n \geq \rho^*$  can be detected if and only if it induces at least one of the TFCs beyond their regions of uncertainty.

*Proof:* By converse of statement in Theorem 1 we have Theorem 2.

*Corollary 2:* If  $\eta_i$  were the event that the  $i^{th}$  coefficient is in its region of detectability ( $\Gamma_i$ ), then the event  $\eta$  of at least one of the coefficients being in their region of detectability is given by

$$\eta = \bigcup_{i=0}^{\lambda+\mu+1} \eta_i \quad (21)$$

Equation (22) follows from (21) as we have  $\eta_i \subseteq \eta$ .

$$\wp(\eta) \geq \wp(\eta_i) \quad (22)$$

By *definition 5* we have  $FC_{C_k} = \wp(\eta_i)$  and  $FC = \wp(\eta)$  therefore on evaluating the integral in (20) we get

$$FC \geq FC_{C_k} = \left\{ \prod_{i=1}^N Q\left(\frac{-p_{in}}{\sigma}\right) \right\} - \left\{ Q\left(\frac{-\alpha}{\sigma}\right) - Q\left(\frac{\alpha}{\sigma}\right) \right\}^N \quad (23)$$

The result in (23) is the lower bound on FC. On substituting typical values for nominal parameter values ( $p_{in} = 5\sigma$  and  $\pm\alpha = \pm 3\sigma$ ), we get (24). Note that (24) is independent of  $\epsilon$ .

$$FC \geq FC_{C_k} = 1 - 0.8427^N \quad (24)$$

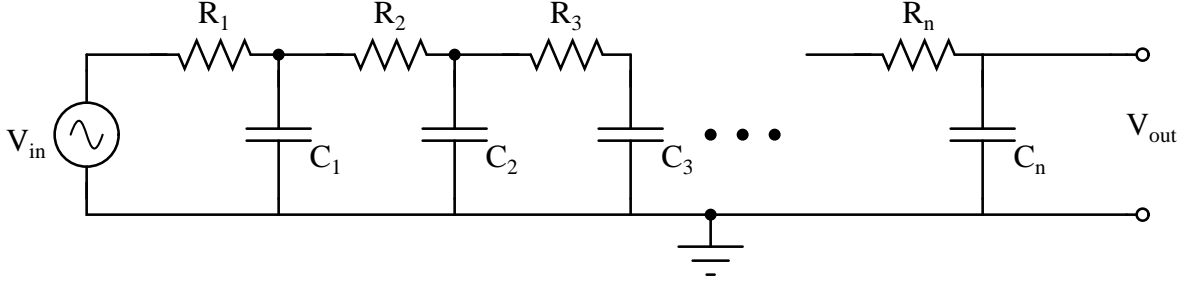


Fig. 2. RC ladder network of  $n$  stages.

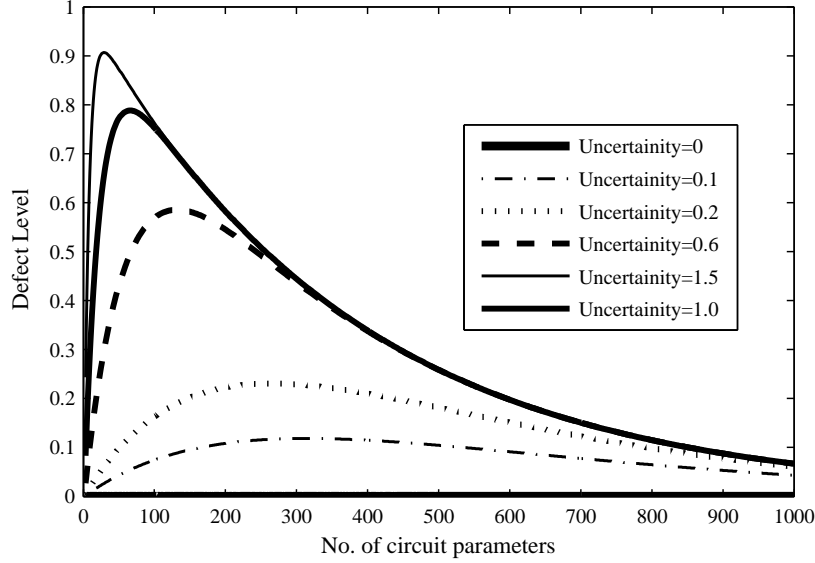


Fig. 3. Defect level (DL) as a function of number of components ( $N$ ).

#### IV. EXPERIMENTAL RESULTS

We present plots of DL in (15) against the number of circuit parameters ( $N$ ) in Figure 2 and against the ratio of coefficient of uncertainty ( $\epsilon$ ) to standard deviation ( $\sigma$ ) in Figure 3. Also plotted in Figure 4 and Figure 5 are the simulated values of DL and FC for different  $N$  and  $\epsilon = 0.1$ . RC ladder networks of varying sections as shown in figure 2 depending on number of components ( $N$ ) were subjected to TFC based test. Note that the number of components is twice the number of RC stages( $n$ ). The transfer functions of RC ladders for arbitrary number of sections is well studied [14], [15]. This was used to find the actual transfer function. Out of this one of the coefficients was subjected to non-linear optimization to find MSDF for each of the parameters. NMSDF for each of the parameters was found based on the coefficient of uncertainty desired. Here we took  $\epsilon = 0.1$  and single parametric faults were then injected and simulated. The parametric faults greater than MSDF but lesser than NMSDF which passed the test were then used to find the DL. FC was similarly found based on fraction of all the faults that failed the test. It can be seen that there is good coupling between simulated values and theoretically derived bound for both DL and FC. It is interesting to note the following inferences from the plots in Figures 2 and 3.

- The DL initially increases and then decreases with increasing number of components in the circuit. The initial increase can be attributed to the fact that increasing the component count leads to greater probability of fault masking due to departures of component values in opposite directions. This would lead to greater probability of fault being masked. However, contrary to intuition, component values beyond a certain threshold result in decrease of DL. This is a manifestation of stochastic resonance, in that, a circuit with large number of components can aid those sections of circuit that induce faults in opposite directions, thereby resulting in a lower DL.
- In Figure 3, we can see that for medium number of components, DL is relatively unchanged for larger coefficients of uncertainty. On the contrary  $\epsilon$  has to be made far smaller to gain in DL.
- FC monotonically increases with the number of components as in Figure 4. An increase in number of components implies

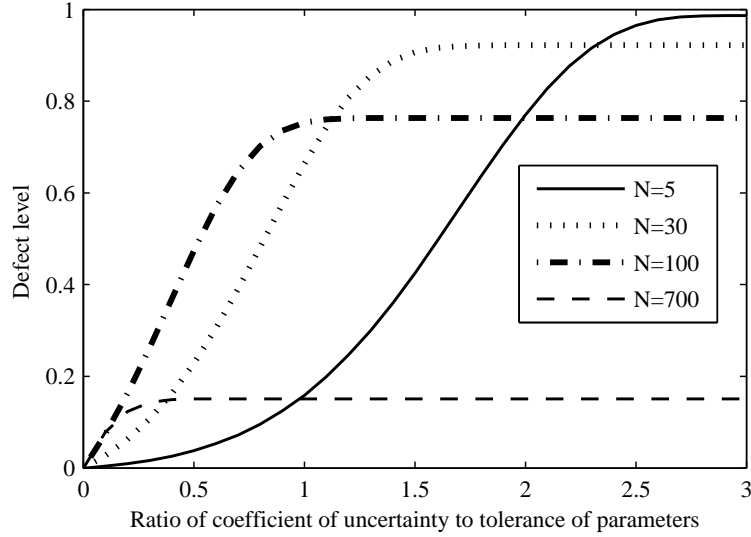


Fig. 4. Defect level (DL) plotted against ratio of coefficient of uncertainty to standard deviation ( $\frac{\xi}{\sigma}$ ).

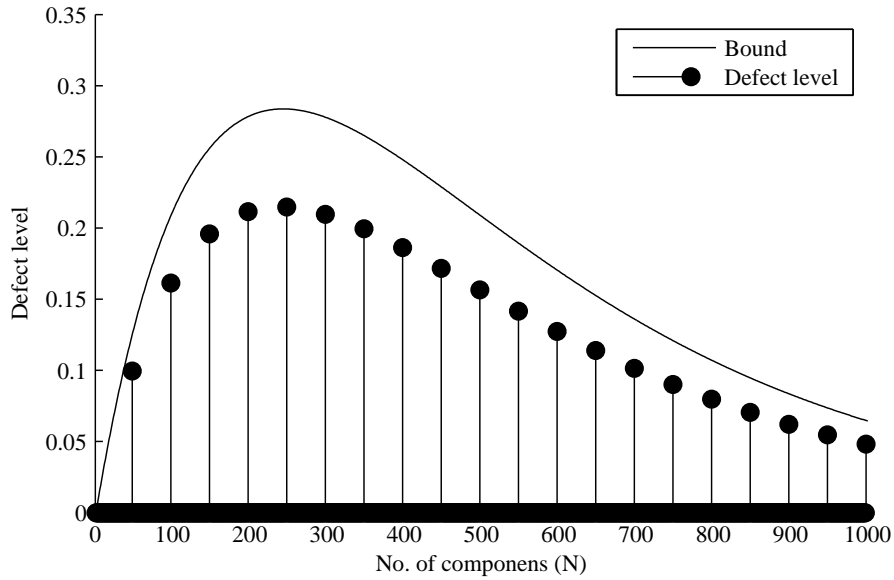


Fig. 5. Comparison of defect level bounds with simulated value ( $\frac{\xi}{\sigma} = 0.1$ ) for RC ladder network.

a greater observability for each coefficient. Increased observability is due to the fact that every added component need not increase the count of number of coefficients. For example, a resistor added may not increase the order of the circuit. This leads to more circuit parameters per coefficient and hence an increased observability. This in turn increases FC as more parameters now have a bearing on circuit TFCs.

To further validate the bounds derived, we simulated and tested TFC based approach on benchmark circuits proposed and maintained by Kondagunturi et al. [12]. These are spice models from ITC'97 benchmark circuits and Statistical Fault Analyzer (SFA) based models proposed by Epstein et al. [16]. The fault model chosen by us for parametric faults(soft faults) is  $\sigma$  deviation from nominal value and for catastrophic faults we used open/short faults. To obtain the FC values, we Monte Carlo simulated each circuit for single parametric faults of size greater than or equal to  $\sigma$  and then found out the set of faults that were uncovered by TFC based approach for the chosen value of coefficient of uncertainty. Here we chose  $\frac{\xi}{\sigma} = 0.1$ . The computed and simulated values of DL and FC for each of the benchmark circuits is tabulated in Table I and II respectively.

TABLE I  
DEFECT LEVEL ON BENCHMARK CIRCUITS FOR  $\frac{\epsilon}{\sigma} = 0.1$

Circuit	Source	Component Count					Defect Level(%)	
		Transistor	Opamp	Resistor	Capacitor	Total(N)	Computed	Simulated
Operational Amplifier #1	ITC '97a	8	-	2	1	11	6.51	5.69
Continuous-Time State-Variable Filter	ITC '97b	-	3	7	2	12	5.89	5.23
Operational Amplifier #2	ITC '97c	10	-	-	1	11	6.51	5.69
Leapfrog Filter	ITC '97d	-	6	13	4	23	1.38	1.33
Digital-to-Analog Converter	ITC '97e	16	1	17	1	35	0.21	0.2
Differential Amplifier	SFAa	4	-	5	-	9	7.72	6.43
Comparator	SFAb	-	1	3	-	4	7.78	3.75
Single Stage Amplifier	SFAc	1	-	5	-	6	8.73	6.17
Elliptical filter	SFAd	-	3	15	7	25	1.02	0.99
Low-Pass Filter	Lucent1	-	1	3	1	5	8.51	5.30

## V. DISCUSSION

We now introduce the “simulation-optimization” tradeoff that results in a typical TFC based analog circuit test scenario. For circuits with more than ten components, the time required for simulation is much less compared to optimization of TFC with a coefficient of uncertainty ( $\epsilon > 0.1$ ). However, for smaller component count (e.g.,  $N = 12$  resistors and capacitors) and uncertainty coefficient ( $\epsilon = 0.07$ ) simulation has to be carried out at a large number of points. The number of points where simulation must be carried out to realize a lower  $\epsilon$  increases steeply for values of  $\epsilon \leq 0.07$  (e.g., points along edges and planes of hypercube enclosing the coefficient instead of just the vertices are now to be simulated) and optimization turns out to be computationally cheaper than simulation. The plot of CPU time required in seconds against uncertainty for both optimization and simulation is plotted in Figure 6. Note that the time required for optimization is same regardless of the value chosen for  $\epsilon$ , as optimizing results in actual MSDF where  $\epsilon = 0$ . Time required for simulation decreases exponentially with increasing  $\epsilon$ . Thus there is a tradeoff between the number of circuit parameters, coefficient of uncertainty (and in turn DL) that has to be evaluated before choosing to simulate or optimize a circuit as the computational overheads with wrong choice can be substantial.

## VI. CONCLUSION

We have derived the bounds for DL and FC possible in transfer coefficient based analog circuit test. The results were generalized for circuits with arbitrarily large number of components. We observed that a higher component count yields lower DL and higher FC in transfer function coefficient (TFC) based approach for testing linear analog circuits. Further, the bounds were validated on several benchmark circuits. It was found that the derived bounds were asymptotically tight. A possible strategy for usage of simulation versus non-linear optimization to find the minimum size detectable faults in coefficient based testing was presented. We found that for lower DLs it is computationally more expensive to simulate, instead, we may use non-linear optimization. In future, we want to find the bounds on DL and FC for the generalized coefficient based test method reported in [17].

TABLE II  
 FAULT COVERAGE ON BENCHMARK CIRCUITS FOR  $\frac{\epsilon}{\sigma} = 0.1$

Circuit	Source	Component Count					Fault Coverage(%)	
		Transistor	Opamp	Resistor	Capacitor	Total(N)	Computed	Simulated
Operational Amplifier #1	ITC '97a	8	-	2	1	11	84.78	85.31
Continuous-Time State-Variable Filter	ITC '97b	-	3	7	2	12	87.17	87.66
Operational Amplifier #2	ITC '97c	10	-	-	1	11	84.78	85.31
Leapfrog Filter	ITC '97d	-	6	13	4	23	98.05	98.19
Digital-to-Analog Converter	ITC '97e	16	1	17	1	35	99.75	99.78
Differential Amplifier	SFAa	4	-	5	-	9	78.57	79.18
Comparator	SFAb	-	1	3	-	4	49.57	50.21
Single Stage Amplifier	SFAc	1	-	5	-	6	64.19	64.87
Elliptical filter	SFAd	-	3	15	7	25	98.61	98.72
Low-Pass Filter	Lucent1	-	1	3	1	5	57.50	58.18

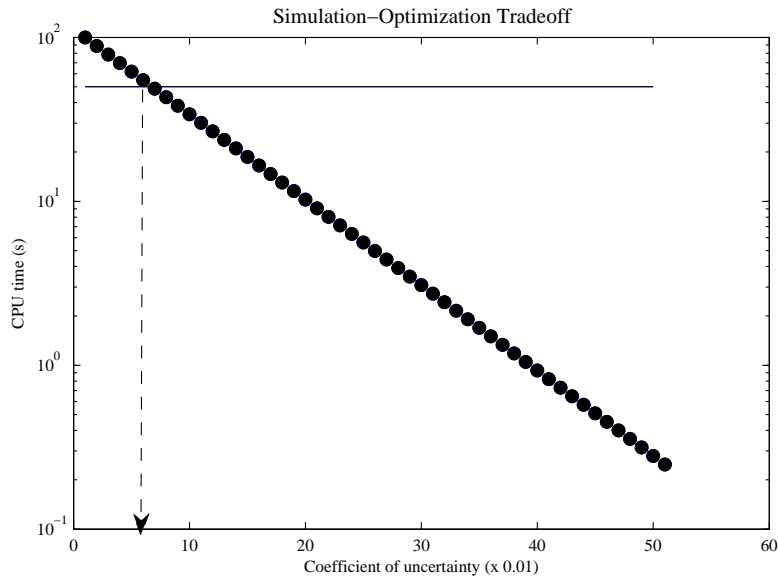


Fig. 6. CPU time to compute NMSDF by simulation versus coefficient of uncertainty,  $\epsilon$ .

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