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All-Digital Replica Techniques for Managing Random Mismatch in Time-to-Digital Converters

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***Abstract*—We propose replica techniques with statistical post processing to improve integral non-linearity (INL) and code distribution performance of time-to-digital converters (TDC). We consider three different types of TDC namely: vernier delay line, multi-resolution, and ring oscillator based. We show that using a replica delay line with additional digital processing at the output, one can achieve better INL and code distribution (at every code) in each of the TDC architectures. The quantum of improvement is only limited by the additional hardware that is to be added, and can be traded for arbitrarily high improvements in INL and code distribution.**

I. Introduction

Time-to-digital converters (TDC), by definition, convert a finite time interval into quantized values, which can then be stored or processed on a digital computer, much in the same way as an analog-to-digital converter would convert voltage levels into quantized values to be stored or processed by a digital computer. Typical applications of TDC include phase detectors in all-digital phase locked loops [4], laser range finders, measuring instruments, and space science applications. TDC, in its most generic form, consists of a network of delay cells (buffers or inverters) connected in cascade to generate varied amounts of delay, which serves as a yardstick for measuring the relative time differences between the signals. The pair of signals between which delay is to be measured is applied at the input. The resolution of the TDC is governed by the delay of the individual delay cell, while the range or the maximum delay value that can be measured by TDC is determined by the number of delay cells in the cascade.

The main difficulty in practical realization of high resolution TDC is the random mismatch among the delay cells due to variability in the manufacturing process that can contribute to an increase in integral non-linearity (INL), and variance in code distribution, that is, the problem of non-unique (or multiplicity) of output digital code for same or similar time difference between the pair of input signals. In order to correct for such random mismatch, several methods [6] have been proposed, that try to *tune* the delays of individual delay cells post fabrication, using "knobs" such as transistor widths (inside buffers), changing transistor thresholds by body biasing, and supply voltage biasing. But all these techniques suffer from the fact that they, (1) attempt to change delays of individual cells causing an increased calibration time and (2) are analog in nature and would therefore need good precision in controlling the "knobs." To overcome these challenges, what is attempted in this paper is an all-digital post processing scheme, without actually changing the delay of individual cells, instead, fabricating additional cascades of delay cells that are a replica of the main delay line and serve to provide additional outputs that are then used to compute a statistically smoothed final output. We investigate three methods of statistical post-processing namely – mean, median and mode of the outputs of individual delay lines. Such a statistically smoothed output is found to improve variance in code distribution and INL to arbitrary levels that is only limited by the amount of additional hardware to be added to the original circuitry.

The paper is organized as follows. Section II describes the proposed replica technique used on a vernier delay line TDC, along with the related performance improvements in each case. Section III discusses the trade-off involved in performance improvement and area overhead of the proposed replica techniques. In the same section, we also discuss the implementation of proposed replica delay line scheme on two other TDC architectures, namely multi-resolution and ring oscillator based TDC. Section IV concludes the paper.

II. Vernier Delay Line TDC

The delay chain of buffers [1] and the Vernier delay line [3], [2] are well-known methods to realize a TDC. In the delay chain shown in Fig. 1, the rising edge of the Start signal propagates through the chain of buffers; when the rising edge of the Stop signal arrives, a flip-flop samples the output of each buffer and produces a thermometer code that locates the relative time interval. However, this simple scheme cannot resolve the time interval better than a single buffer delay. On

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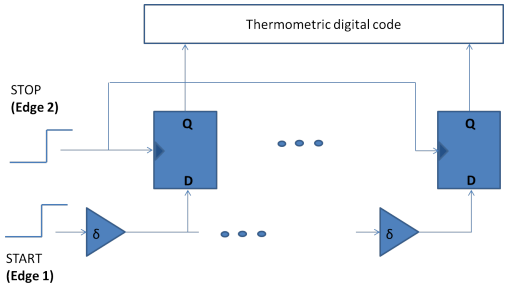

Fig. 1. Generic delay line TDC producing thermometric output.

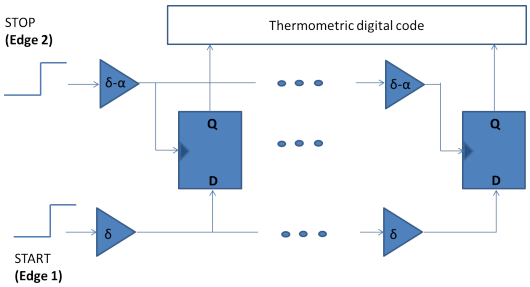

Fig. 2. Vernier delay line TDC producing thermometric output.

the other hand, using the delay difference between unequal buffers, the Vernier delay line in Fig. 2 can resolve more finely, but its area increases linearly with the resolution, and *the devices must match more tightly.* The main concern is in compensating for the mismatch that exists among the delay elements. We use the replica delay line for compensating mismatch in individual delay cells in both the generic delay line TDC and in the vernier delay line TDC architecture. Fig. 3 shows a replica delay line added to the original TDC with the intention of generating additional outputs that can serve the cause of computing mean, median, and mode of the outputs. In the subsequent section we will dwell upon how various averaging schemes such as mean, median and mode used for compensating for the delay mismatch in the vernier delay line TDC.

A. Output Calibration using Averaging

Averaging operation of n variables $v_1, \cdots, v_n$ is mathematically defined as

$$\hat{v} = \frac{1}{N}\Sigma_{i=1}^{N} v_i \tag{1}$$

This is implemented digitally as a serial accumulator followed by a divider. The output of the divider gives an averaged output that is used as the modified output code of the TDC. During the calibration phase of the TDC, for all possible delays (encompassing the entire range) of inputs, the multiplexer shown in Fig. 3 is used to select one of the delay line's output to the D inputs of the flip flops, which is cyclically repeated for all the delay lines used. The final value is computed as the average digital output given by 1, where each v_i $\forall i$ is a digital output produced upon selecting the i^{th} delay line. Now the difference between the average code and the code produced

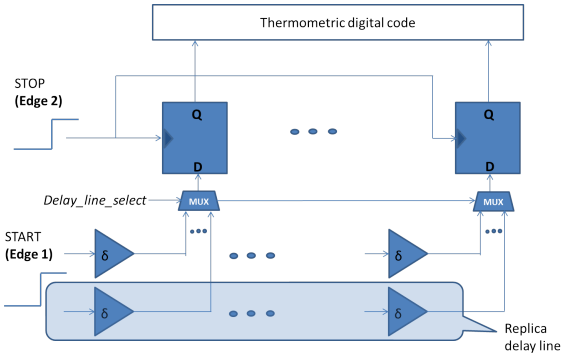

Fig. 3. Proposed TDC producing additional outputs using replica delay lines for compensating delay cell mismatch.

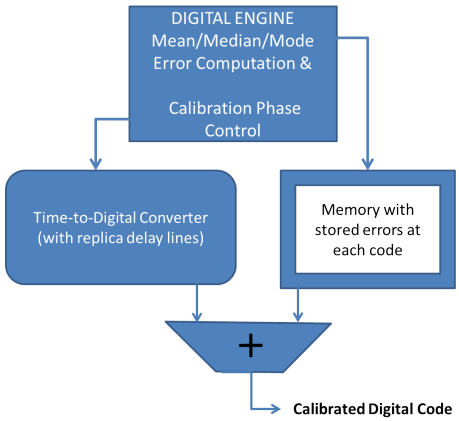

Fig. 4. Block diagram of digital calibration and online compensation scheme.

by the main delay line (say v_1) is computed and is stored in the memory. Note that storing the difference in memory allows usage of small memory since only the relative differences are to be stored. This completes the calibration phase. During the actual working of the TDC, calibration scheme shown in Fig. 4 allows for a rapid mismatch compensation *online*. The adder in Fig. 4 adds the stored differences to the actual output of the main delay line v_1.

Fig. 5 shows the plots of code distribution improvement obtained with averaging compensation of the original TDC code with the replica delay lines. On introducing a delay mismatch of 10% of the nominal delay value of each cell. We observe that the variance in code distribution is improved and the hit rate at code 70 increased from 3860 to 5960 with averaging (alternatively referred to as mean) compensation at the digital code of 70. A total of N=10000 runs was carried out to obtain these numbers.

INL improvement using mean compensation is shown in Fig. 6. Maximum INL is about 13LSBs at 12 bit resolution after mean compensation.

B. Output Calibration using Median

Just as we described the averaging compensation scheme on the Vernier delay line TDC in the previous section, we used another measure of central tendency, namely Median for

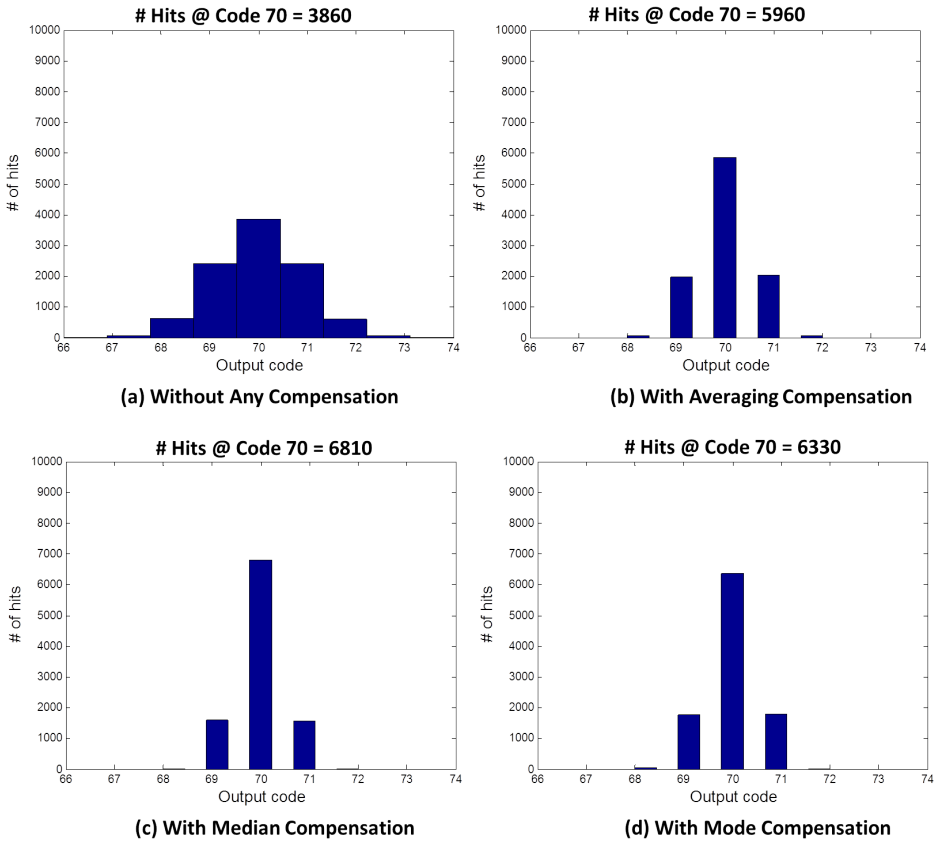

Fig. 5. Code distribution results of different compensation schemes on Vernier delay line TDC.

compensation. Median is defined as the central value of a sorted array of numbers. For a pre-sorted array of n numbers, $v_1 \cdots v_n$, the median, v_{median} is given by Eqn. (2):

$$v_{median} = v_i| \quad i = \lfloor (1+n)/2 \rfloor \tag{2}$$

The reduction in both variance in code distribution (which translates to hit-rate) and INL is marginally better with median compensation than averaging compensation. The results of code distribution using median compensation is shown in part (c) of Fig. 5. The hit rate is improved to 6810 at code 70 using the median compensation. Similarly, the INL improved marginally using the median compensation scheme and is shown in part (c) of Fig. 6. Maximum INL is about 5LSBs at 12 bit resolution after median compensation.

C. Output Calibration using Mode

Mode represents the most repeated value among a set of n integers. This is yet another central tendency that has been known to perform well in systematic mismatch compensation. We use this as yet another measure for mismatch compensation in the vernier delay line TDC. We find that the code distribution and INL performance of mode is between that of mean and median based compensation schemes as can be seen in part (d) of Figs. 5 and 6 respectively. The code hit rate is 6330 out of a total of 10,000 trials at code 70. Magnitude of maximum INL is about 7LSBs at 12 bit resolution.

III. Performance Improvement–Area Trade-off

As we saw in the previous sections, replica delay lines serve to provide additional outputs that can be used by some form of an "averaging" algorithm to estimate actual value of the code, and in the process compensate for degradation in code distribution and INL stemming from random mismatch in the delay cells. The addition of replica delay line, however, comes at a price of increasing area of the TDC. Figure 7 shows the plot of mean variance in code distribution as a function of area overhead for replica lines in the vernier delay line TDC. As can be seen, with the addition of just two replica delay lines, the variance in code distribution and INL can be reduced by more than 45%. However, the reduction in INL and variance in code distribution with area follows the law of diminishing returns, in that, the absolute value of reduction in INL or variance reduces with the increase in redundant hardware. This can be attributed to the variance–hardware overhead relationship, that can be estimated for uncorrelated mismatch by the equation 3:

$$\sigma^2_{code\_distr} = \frac{K}{N}, \tag{3}$$

where K is a proportionality constant, and N is the number of replica delay lines. This result follows from the fact that the mean of N uncorrelated random variables $X_1 \cdots X_N$, each having variance σ^2, results in a new random variable $\bar{X}$ whose

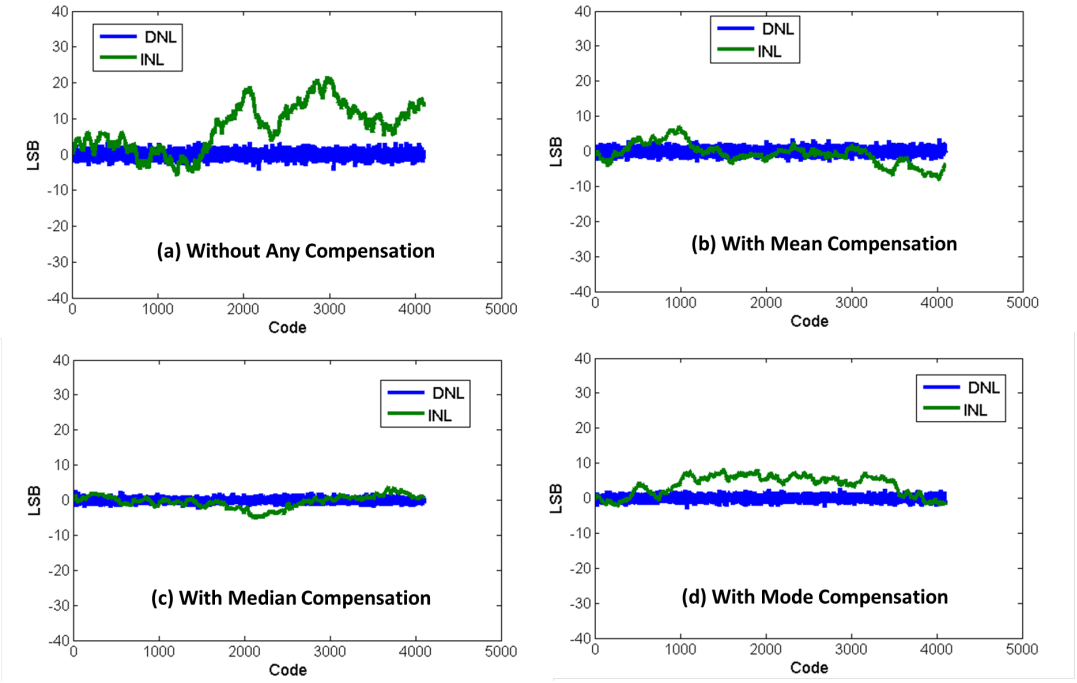

Fig. 6. DNL and INL plots of different compensation schemes on Vernier delay line TDC. Median performs the best among the three statistical compensation schemes in giving the minimal maximum INL across the entire code range.

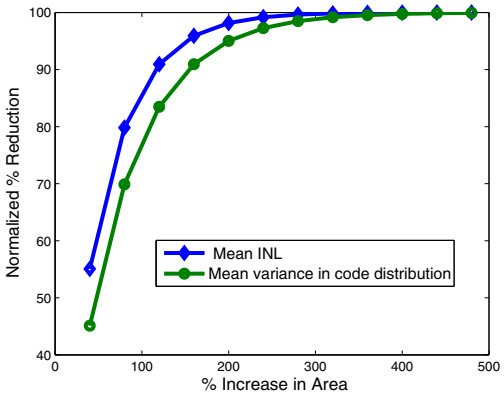

Fig. 7. Percentage reduction in average value of INL (taken across all codes) and mean variance in code distribution plotted as a function of additional area for the Vernier delay line TDC.

variance is given by σ^2/N.

Figs. 8 and 9 show the INL and code distribution variance trade-off with the additional area overhead in case of multi-resolution and ring oscillator based TDC respectively. The values of mean INL and mean variance in code distribution is computed at each code by averaging over 10,000 random samples. It can be seen that in both the cases there is up to 55% reduction in variance in code distribution in both the architectures with an increase of just 50% over the vanilla implementation consisting of no replica delay lines. Mean INL numbers are reduced by more than 70% in both the cases with the same area increase over the vanilla implementation. However as can be seen the percentage reduction in INL or code distribution variance saturates rather quickly.

A. *Multi-resolution TDC*

In a multi-resolution TDC, the outputs are obtained by sampling delay lines, each of which have a different resolution, but the effective resolution of the entire TDC ends up being better than the individual TDC resolution. The details of the architecture is beyond the scope of this paper and we refer the interested reader to reference [5]. We used the replica delay line technique with mean compensation on this type of TDC. We find that the improvement in code distribution and INL is consistent with the expected improvement as seen in the vernier delay line TDC. For example in Fig. 8, we see that for an addition of just 3 delay lines the variance in code distribution is reduced by 55%, while INL is reduced by 70%.

B. *Ring Oscillator Based TDC*

Ring oscillator based TDC uses a closed loop of inverters, instead of an open loop of delay chain (as is the case with normal Vernier delay line TDC). The main advantage of such an approach is virtually very high range, which is only limited by the bit width of the counter, without any loss of resolution. This is very attractive for realizing delay measurement units where time has to be measured at high accuracy but the intended signal delays are very large, for example, pulsed radar for vehicular speed monitoring. The details of implementation of this TDC is beyond the scope of this paper and the interested reader is referred to [7]. Replica delay line technique with mean compensation on ring oscillator based TDC resulted in

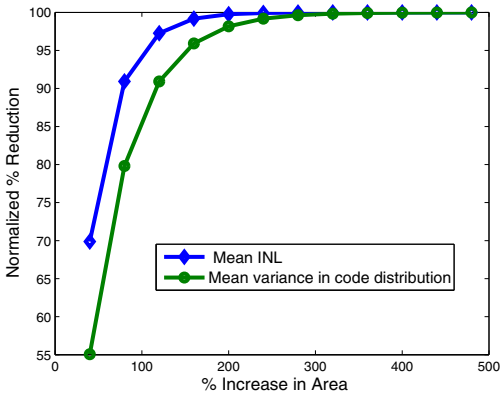

Fig. 8. Percentage reduction in average value of INL (taken across all codes) and mean variance in code distribution plotted as a function of additional area for the multi resolution TDC.

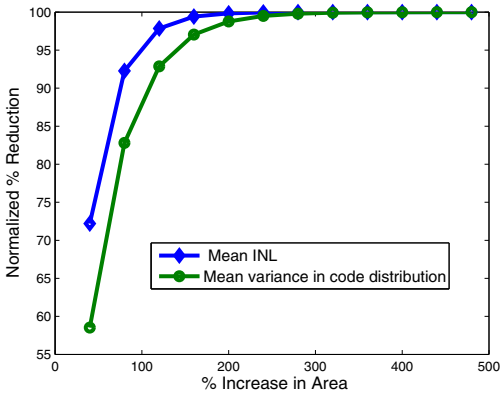

Fig. 9. Percentage reduction in average value of INL (taken across all codes) and mean variance in code distribution plotted as a function of additional area for the ring oscillator based TDC.

an improvement in code distribution and INL that is consistent with the expected improvement as seen in the vernier delay line TDC. For example in Fig. 9, we see that for an addition of just three delay lines the variance in code distribution is reduced by 57%, while INL is reduced by 72%.

IV. Conclusion

We presented replica techniques for improving random mismatch related INL and code-distribution performance in three different TDC architectures. In each case, we were able to obtain improvements of the order of 50-60% with a digital area overhead of about 30%. Further, it was also shown that INL and variance in code distribution due to random delay mismatch of the delay elements can be made arbitrarily small by adding sufficient replica hardware.

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