Dual-Threshold Design of Sub-threshold Circuits

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***Abstract*—Dual threshold voltage (V_{th}) design is a common method for reducing leakage power in above-threshold circuits. This research shows that it is also effective in reducing energy per cycle of sub-threshold circuits. We first study the single-V_{th} design theoretically and by simulations, and find that the energy per cycle is independent of threshold voltage. However, in a dual-V_{th} design, the energy per cycle depends on both threshold voltage and supply voltage. We propose a framework to further reduce energy per cycle below what is possible with a single V_{th}. Given a nominal value for V_{th}, we determine an optimal supply voltage V_{dd} and an optimal higher V_{th}. Application to a 32-bit ripple carry adder shows energy saving of 29% over the single-V_{th} lowest energy.**

I. Introduction

Sub-threshold operation is often referred to as weak inversion operation, where sub-threshold current I_{sub} is the main source of current. It can be summarized as follows [1]:

$$I_{sub} = I_o exp(\frac{V_{gs} - V_{th}}{nV_t})[1 - exp(\frac{-V_{ds}}{V_t})] \quad (1)$$

where

$$I_o = \mu C_{ox} \frac{W}{L}(n-1)V_t^2 \quad (2)$$

μ is effective mobility, C_{ox} is oxide capacitance, W is transistor width, L is transistor length, V_t is thermal voltage, V_{gs} is gate-source voltage, V_{ds} is drain-source voltage, V_{th} is threshold voltage and n is sub-threshold slope.

Sub-threshold circuits are expected to receive increasing attention in the coming years since the minimum energy CMOS operation occurs in the sub-threshold region [2]. In other words, the optimal supply voltage (V_{ddopt}) is typically below V_{th} when minimum energy is achieved. As the supply voltage scales down into the sub-threshold region, due to the exponential relation between V_{gs} and I_{sub}, circuit delay increases exponentially which causes significant increase in the fraction of leakage energy. On the other hand, dynamic energy decreases relatively slower, i.e., quadratically as supply voltage scales down. Minimum energy point is reached when dynamic energy equals leakage energy.

II. Single-V_{th} Sub-threshold V_{dd} Design

We establish that energy is independent of V_{th} for a single-V_{th} and sub-threshold V_{dd} design. However, it is feasible to make the circuit faster without increasing the energy per cycle (EPC) by decreasing V_{th}. An analytical expression for EPC can be written as,

$$\begin{aligned} E &= E_{dyn} + E_{leak} = \frac{1}{2}C_{eff}V_{dd}^2 + I_{leak}V_{dd}T \\ &= \frac{1}{2}C_{eff}V_{dd}^2 + I_o exp(\frac{-V_{th}}{nV_t})\ V_{dd}\ \frac{l\ C_g V_{dd}}{I_o exp(\frac{\frac{V_{dd}}{2} - V_{th}}{nV_t})} \end{aligned} \quad (3)$$

TABLE I. PTM 32nm [3] V_{th} calculated by HSPICE [4].

Model	NMOS	PMOS
High performance (HP)	0.328 V	−0.291 V
Low performance (LP)	0.549 V	−0.486 V

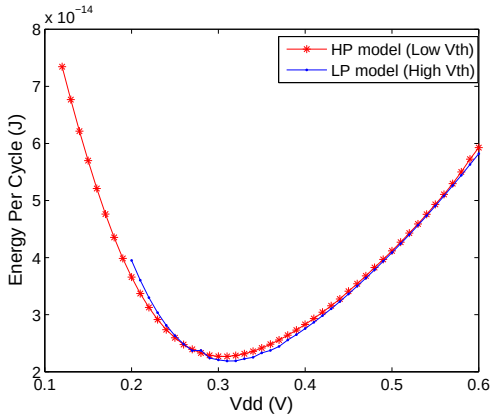

Fig. 1. Random-vector simulation by HSPICE [4] for energy per cycle (EPC) for 32-bit RCA single V_{th} designs in PTM 32nm CMOS [3] with $W_n = 5L$ and $W_p = 12L$.

where C_{eff} is average switched capacitance per clock cycle in the circuit, C_g is gate capacitance of a characteristic inverter, l is the length of the critical path in terms of characteristic inverters and T is the clock period. In addition, if we assume that $V_{ds} > 3V_t$, so that $1 - exp(\frac{-V_{ds}}{V_t}) \approx 1$, then we arrive at the following expression for energy,

$$E = \frac{1}{2}\ C_{eff}\ V_{dd}^2 + \frac{l\ C_g V_{dd}^2}{exp(\frac{V_{dd}}{2nV_t})} \quad (4)$$

From (4) we see that the V_{th} factor is canceled out in the energy expression which means V_{th} has no effect on EPC. We verified this theory by simulating a 32-bit ripple carry adder (RCA) in HSPICE. We used PTM 32nm technology [3] which offers two models, a low performance (LP) model with high V_{th} and a high performance (HP) model with low V_{th}. Table I lists the V_{th} values calculated at nominal $V_{dd} = 0.9V$ by HSPICE [4]. The EPC for the two single threshold voltage circuits as functions of V_{dd} computed by HSPICE [4] (simulating random input vectors) are shown in Figure 1. The red curve is for low V_{th} and the blue curve is for high V_{th}. We notice that EPC for the two designs remain practically same over the sub-threshold supply voltage range $V_{dd} = 0.12$V to $V_{dd} = 0.4$V. As V_{dd} scales down EPC decreases reaching a minimum at the same V_{ddopt} just above 300mV. When V_{dd} decreases further, EPC increases as leakage energy dominates. Logic operations breakdown earlier, at about $V_{dd} = 200$mV, for high V_{th}. The low V_{th} design continues to work at lower V_{dd}.

III. Dual-V_{th} Sub-threshold V_{dd} Design

In this section, we demonstrate the effectiveness of dual-V_{th} technique as a method to reduce EPC for sub-threshold

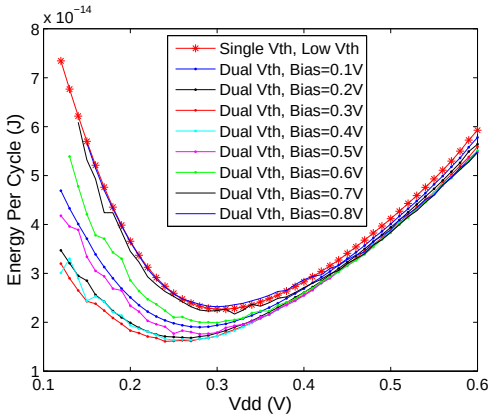

Fig. 2. Random-vector simulation by HSPICE [4] for energy per cycle (EPC) for 32-bit RCA single and dual-V_{th} designs in PTM 32nm CMOS [3] with $W_n = 5L$ and $W_p = 12L$.

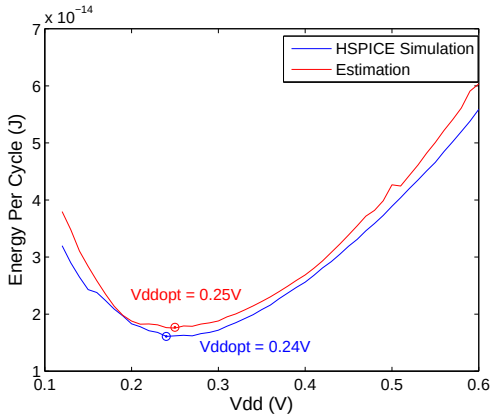

Fig. 3. Random-vector HSPICE [4] simulation results vs. estimation results for energy per cycle (EPC) for 32-bit RCA dual-V_{th} design with reverse body bias voltage = 0.3V.

circuits. Our dual-V_{th} design keeps circuit speed the same as single-V_{th} design with low V_{th}, while reducing the leakage power via assigning high V_{th} to appropriate gates. We use a gate-level slack based algorithm [5], [6] to generate dual-V_{th} design, consisting of following steps:

1) Assign low V_{th} to all gates.
2) Run static timing analysis (STA) to calculate slack [5] for each gate and circuit delay (T) for every V_{dd} and high V_{th} condition.
3) Using gate slacks assign gates to high V_{th} such that critical path delay does not degrade.
4) Estimate EPC, V_{ddopt} and an optimal high V_{th} level which gives the lowest EPC. To estimate EPC, we sum up the energy of all gates, $i = 1, \cdots n$. as shown below, where C_{eff} and P_{leak} are obtained from HSPICE [4] for basic logic gates under varying V_{dd}, V_{th} and fan-out conditions.

$$E = \sum_{i=1}^{n} E_i = \alpha \; C_{eff,i} \; V_{dd}^2 + P_{leak,i} \; T \qquad (5)$$

5) Simulate dual-V_{th} design [4] and compare EPC, V_{ddopt} and optimal high V_{th}.

Figure 2 shows how EPC is lowered via optimized dual-V_{th} design. Supply voltage ranges from 0.12V to 0.6V and we apply reverse body bias voltages to the example circuit in the range between 0.1V to 0.8V. For any given V_{dd}, EPC decreases as bias voltage increases until it reaches a lower bound. Then it starts to increase slowly, finally reaching the same value as the single-V_{th} design. The lowest minimum energy occurs when the bias voltage equals 0.3V. The minimum EPC in Figure 2 is 1.610×10^{-14}J at $V_{ddopt} = 0.24$V. The corresponding critical path delay is $T = 1.2134\mu$s, resulting in a clock frequency of 0.8241MHz.

In comparison, for the two single-threshold designs of Figure 1 the minimum EPC is 2.268×10^{-14}J at $V_{ddopt} = 0.31$V. For low V_{th} circuit, $T = 250.11$ns or clock frequency = 3.998MHz, and for high V_{th} circuit, $T = 35.835\mu$s or clock frequency = 27.9kHz. Thus, EPC for the dual-V_{th} circuit is 29.1% lower than that for either of the single-V_{th} circuit. The speed of the dual-V_{th} circuit is between the speeds of the two single-V_{th} circuits.

Figure 3 compares estimated EPC of dual-V_{th} designs with HSPICE [4] simulation. The average error between the estimation and simulation is 6.99%. The error may result from simplifications made in the framework. For example, we assume that fan-out gates are always low V_{th} gates when calculating output capacitance of the driving gate in HSPICE [4]. That is, when a gate drives high V_{th} gates, the difference in output capacitance is considered negligible.

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IV. Conclusion

We use the energy per cycle (EPC) as a measure of efficiency of a CMOS circuit. It is known that minimum EPC for CMOS circuits occurs when V_{dd} has a sub-threshold value. We show that this optimum operation remains unchanged as the threshold voltage (V_{th}) of devices is varied in a single threshold circuit. The reason is that an increase of V_{th} increases the delay and decreases the leakage current in similar proportions. We find a new minimum for EPC of the sub-threshold V_{dd} circuit achieved by our dual-V_{th} design. As an example, EPC of a 32-bit ripple carry adder in 32nm CMOS is lowered by 29% over its single threshold version.

References

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