LNA Test: A Polynomial Coefficient Approach

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Outline

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To Develop an Analog Circuit Test Scheme

- Suitable for large class of circuits

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Our Idea

Taylor series expansion of circuit function in terms of magnitude of input v_{in} at a frequency

$$v_{out} = f(v_{in})$$
$$v_{out} = f(0) + \frac{f'(0)}{1!} v_{in} + \frac{f''(0)}{2!} v_{in}^2 + \frac{f'''(0)}{3!} v_{in}^3 + \cdots + \frac{f^{(n)}(0)}{n!} v_{in}^n + \cdots$$

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Ignoring the higher order terms we have

$$v_{out} \approx a_0 + a_1 v_{in} + a_2 v_{in}^2 + \cdots + a_n v_{in}^n$$

where every $a_i \in \Re$ and is bounded between its extreme values for

$$a_{i,\min} < a_i < a_{i,\max} \; \forall i \; 0 \leq i \leq n$$

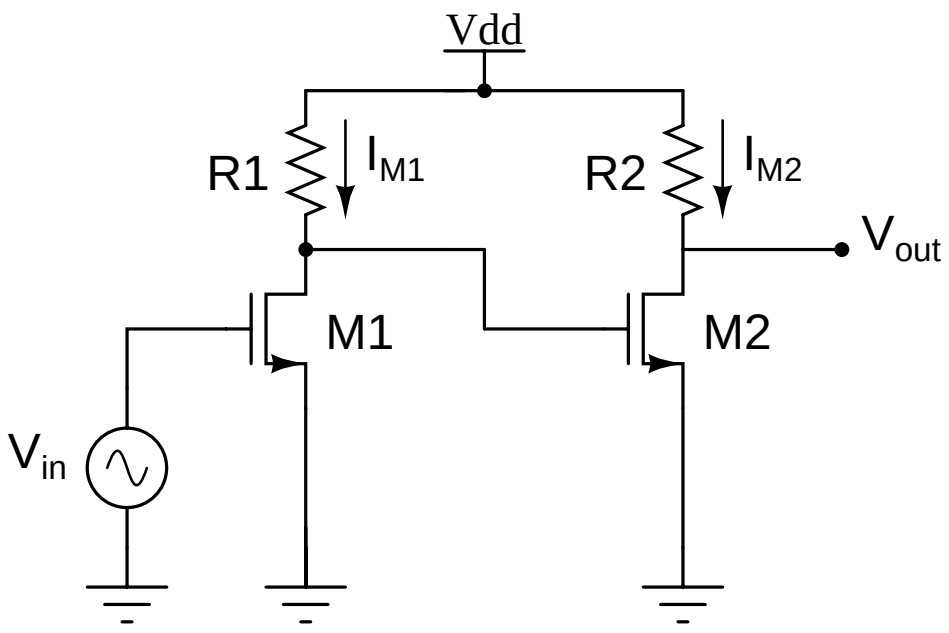
Our Idea (Contd..)

In a Nutshell

- Find the V_{out} v/s V_{in} relationship at frequencies of interest (Eg.: Cutoff, fundamental)
- Compute the coefficients of fault-free circuit
- Repeat the same for CUT by curve fitting the I/O response
- Compare each of the obtained coefficients with fault-free circuit range
- Classify CUT as Good or Bad

Cascaded Amplifiers

An Example



Two stage amplifier with 4th degree non-linearity in V_{in}

$$v_{out} = a_0 + a_1 v_{in} + a_2 v_{in}^2 + a_3 v_{in}^3 + a_4 v_{in}^4$$

Polynomial Coefficients

$$a_0 = V_{DD} - R_2 K \left(\frac{W}{L}\right)_2 \left[\begin{array}{l} (V_{DD} - V_T)^2 + R_1^2 K^2 \left(\frac{W}{L}\right)_1^2 V_T^4 \\ -2(V_{DD} - V_T) R_1 \left(\frac{W}{L}\right)_1 V_T^2 \end{array} \right]$$

$$a_1 = R_2 K \left(\frac{W}{L}\right)_2 \left[4 R_1^2 K^2 \left(\frac{W}{L}\right)_1^2 V_T^3 + 2(V_{DD} - V_T) R_1 K \left(\frac{W}{L}\right)_1 V_T \right]$$

$$a_2 = R_2 K \left(\frac{W}{L}\right)_2 \left[2(V_{DD} - V_T) R_1 K \left(\frac{W}{L}\right)_1 - 6 R_1^2 K^2 \left(\frac{W}{L}\right)_1^2 V_T^2 \right]$$

$$a_3 = 4 V_T K^3 \left(\frac{W}{L}\right)_1^2 \left(\frac{W}{L}\right)_2^2 R_1^2 R_2$$

$$a_4 = -K^3 \left(\frac{W}{L}\right)_1^2 \left(\frac{W}{L}\right)_2^2 R_1^2 R_2$$

MSDF Calculation

Definition

Minimum Size Detectable Fault (ρ) of a circuit parameter is defined as its minimum fractional deviation to force at least one of the polynomial coefficients out of its fault free range

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Overview of MSDF calculation of R1 with $\mathrm{V_{DD}}$=1.2V, $\mathrm{V_T}$= 400mV, $\left(\frac{W}{L}\right)_1 = \frac{1}{2}\left(\frac{W}{L}\right)_2 = 20$, and $\mathrm{K} = 100\mu\mathrm{A/V^2}$

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Maximize a_0

$$\left\{1.2 - R_{2,nom}(1+y)\left(\begin{array}{l} 2.56\mathrm{x}10^{-3} + R_{1,nom}^2(1+x)^2 1.024\mathrm{x}10^{-7} \\ -5.12\mathrm{x}10^{-4} R_{1,nom}(1+x) \end{array}\right)\right\}$$

subject to a_1, a_2, a_3, a_4 being in their fault free ranges and

$$-\alpha \leq x, y \leq \alpha$$

MSDF Calculation (contd..)

Assuming single parametric faults, ρ for R_1

$$\rho = (1+\alpha)^{1.5} - 1 \approx 1.5\alpha - 0.375\alpha^2$$

MSDF Calculation (contd..)

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MSDF for Cascaded Amplifier with α = 0.05

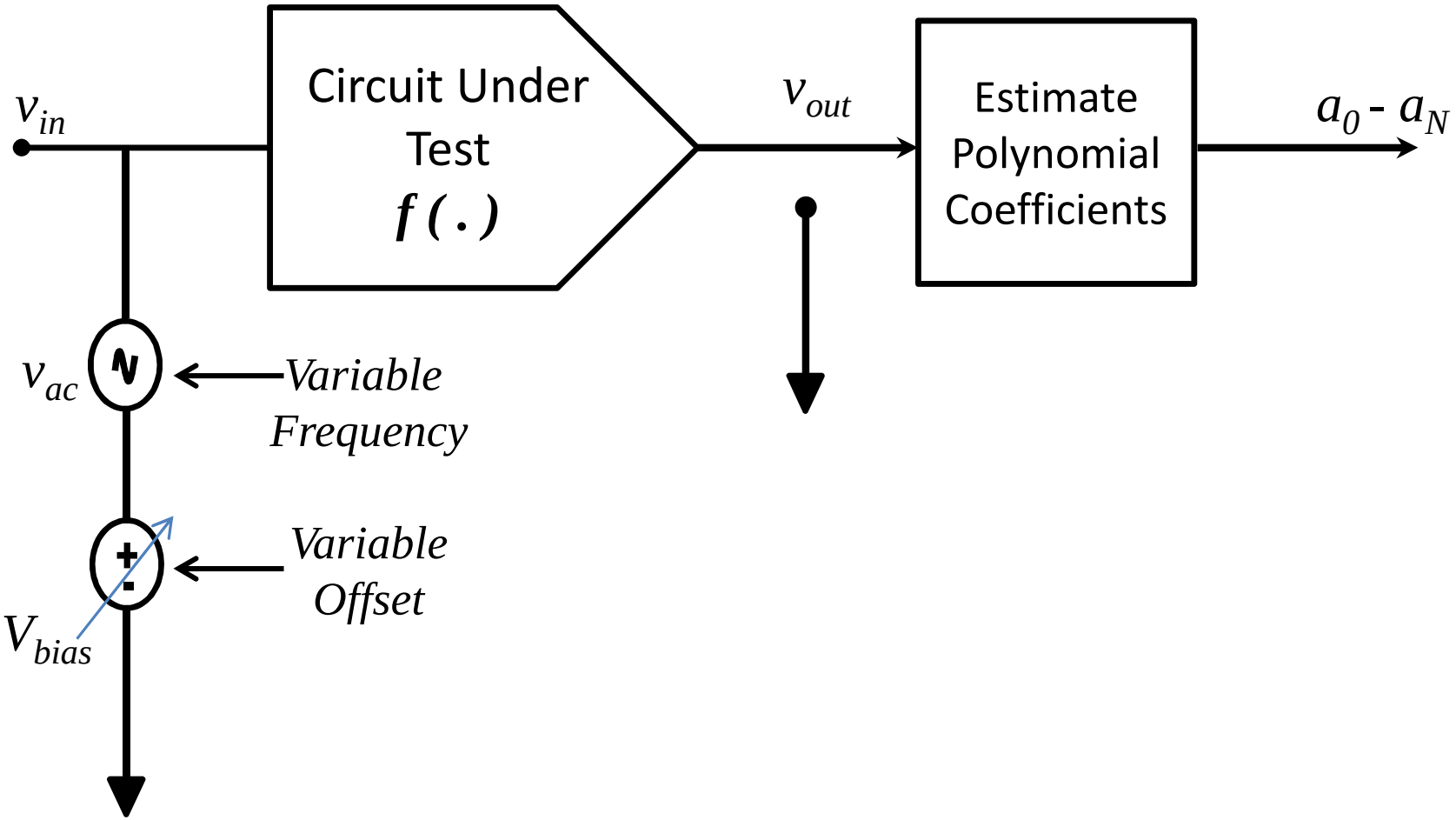
Circuit parameter	%upside MSDF	%downside MSDF
Resistor R_1	10.3	7.4
Resistor R_2	12.3	8.5

Outline

Generalization – Fault Simulation

1. Start
2. Choose a frequency of interest
3. Sweep bias at the input and note corresponding output voltage levels
4. Polynomial curve fit the obtained I/O data – find the coefficient values of fault free circuit
5. Simulate for all parametric faults at the simplex of hypercube
6. Find min-max values of each coefficient (C_i) from $i = 1 \cdots N$ across all simulations
7. Stop

Test Setup


v_{in}
Circuit Under Test
$f(.)$
v_{out}
Estimate Polynomial Coefficients
a_0 - a_N
v_{ac}
Variable Frequency
Variable Offset
V_{bias}

Generalization – Test Procedure

1. Start
2. Sweep bias at the input and note corresponding output voltage levels
3. Polynomial curve fit the obtained I/O data
4. Start with first coefficient
5. Consider next coefficient C_{i+1}
6. $|C_i| > \left|C_{i,max}\right|$ *or* $|C_i| < \left|C_{i,min}\right|$?
   If True go to step 9
7. $i < N$? If True go to step 5
8. Subject CUT to further tests. Stop
9. CUT is faulty. Stop

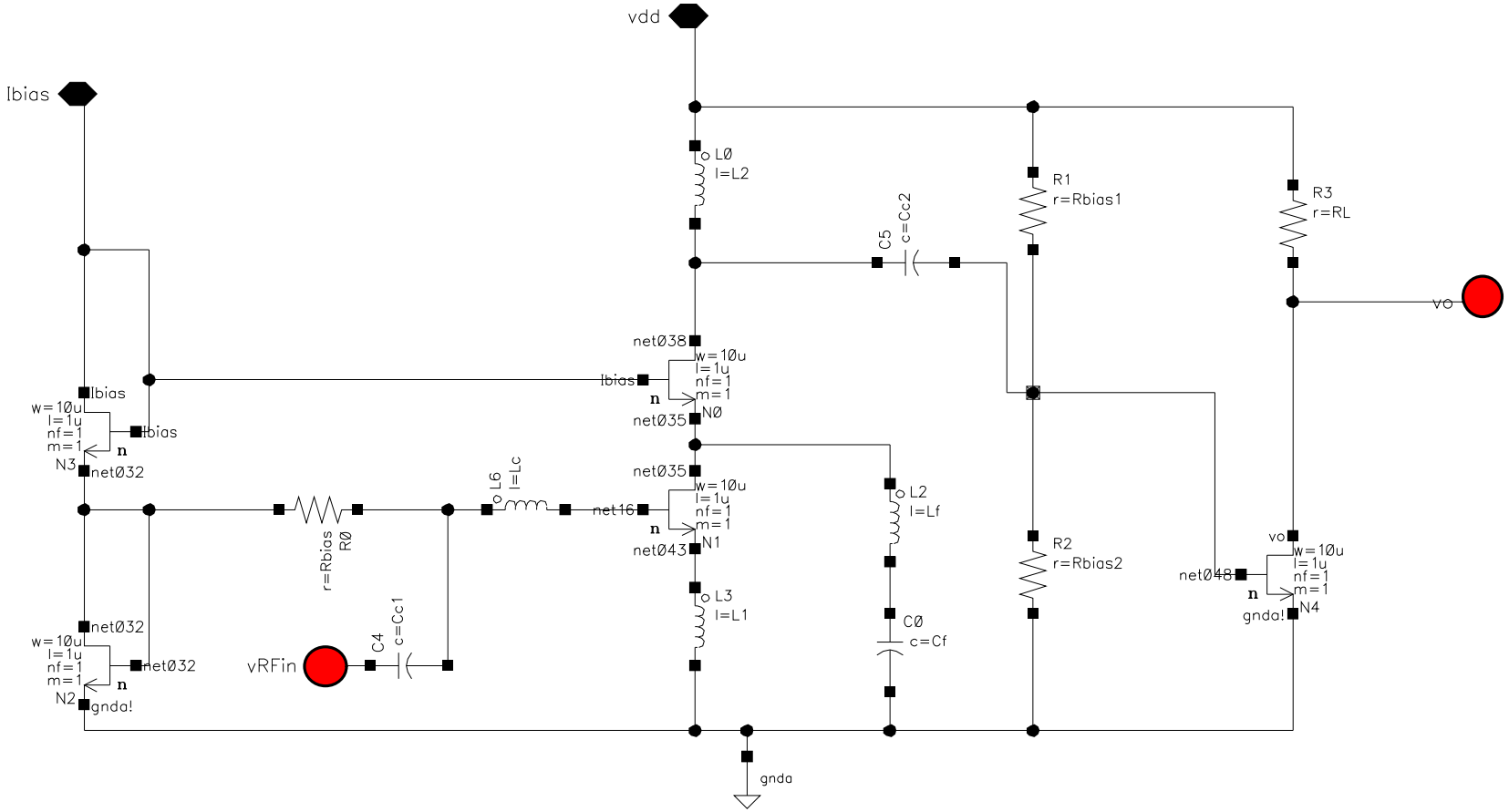
Outline

Low Noise Amplifier

Specifications

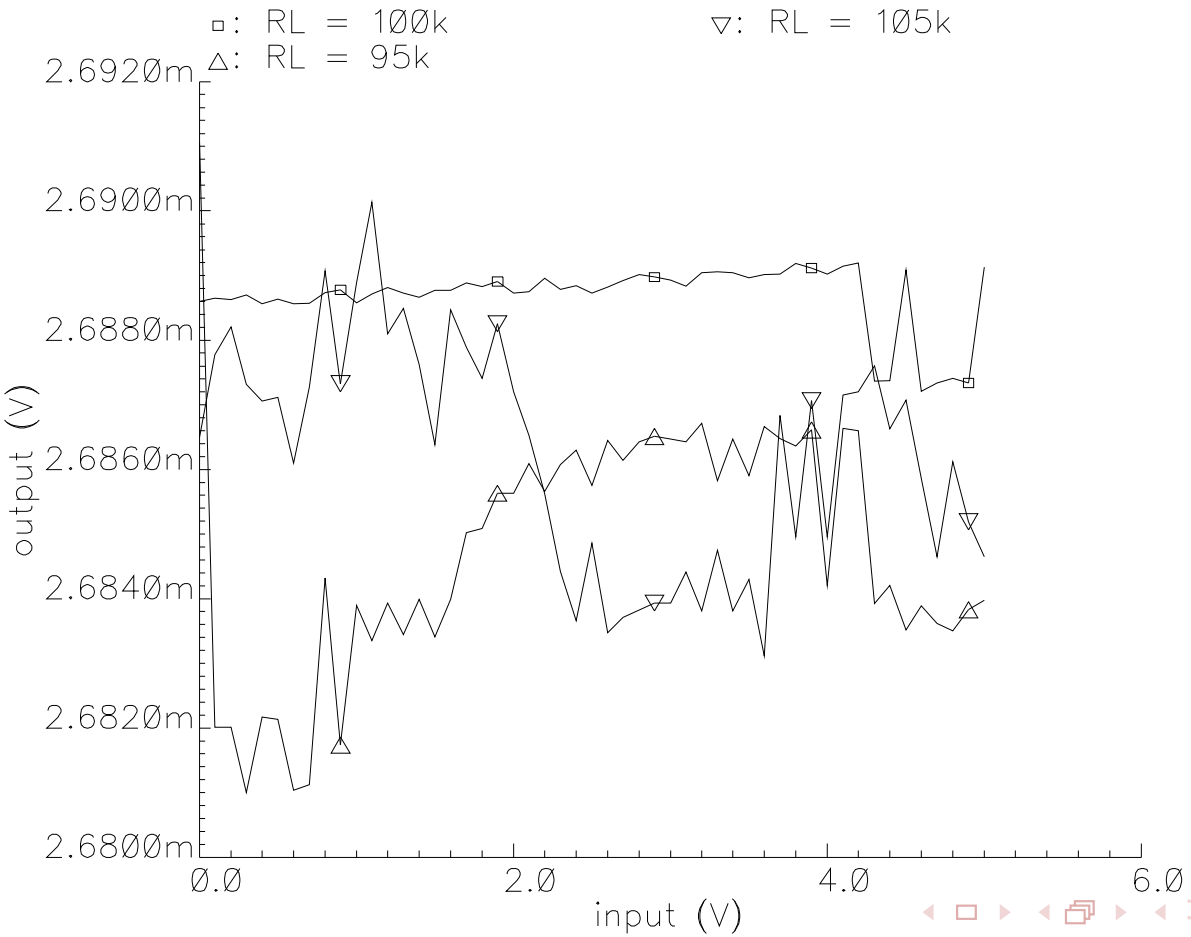
Performance Parameter	Nominal Value
Gain (dB)	16
IIP_3 (dBm)	-18
Noise figure (dB)	9.1
S_{11} (dB)	-16.5

Low Noise Amplifier – Schematic



Results - Output Comparison @ 10GHz

Comparison for parametric fault in $R_L = 100k\ ohm$



Results – Low Noise Amplifier @ 10GHz

Parameter Combinations Leading to Max Values of Coefficients with α = 0.05

Component (ohm, nH, fF)	a_0	a_1	a_2	a_3	a_4	a_5
$R_{bias} = 10$	10	10	10.5	10.5	9.5	10.5
$L_C = 1$	1	0.95	1.05	0.95	1.05	1
$C_{C1} = 100$	95	95	95	95	95	105
$L_1 = 1.5$	1.425	1.5	1.5	1.425	1.575	1.425
$L_2 = 1.5$	1.5	1.425	1.425	1.575	1.5	1.5
$L_f = 1$	1.05	1.05	1.05	1	1.05	1
$C_f = 100$	105	95	95	105	95	95
$C_{C2} = 100$	95	100	105	95	95	95
$R_{bias1} = 100k$	105k	105k	100k	105k	105k	95k
$R_{bias2} = 100k$	105k	95k	100k	95k	95k	95k
$R_L = 100k$	100k	95k	95k	100k	105k	100k

Results – Low Noise Amplifier @ 10GHz

Parameter Combinations Leading to Min Values of Coefficients with α = 0.05

Component (ohm, nH, fF)	a_0	a_1	a_2	a_3	a_4	a_5
$R_{bias} = 10$	10	9.5	9.5	10	10	10
$L_C = 1$	1.05	0.95	0.95	1	1	0.95
$C_{C1} = 100$	100	105	95	100	95	105
$L_1 = 1.5$	1.425	1.5	1.575	1.575	1.575	1.575
$L_2 = 1.5$	1.5	1.575	1.5	1.425	1.425	1.5
$L_f = 1$	1.05	1.05	0.95	0.95	1	0.95
$C_f = 100$	105	95	95	105	105	105
$C_{C2} = 100$	95	105	100	105	95	105
$R_{bias1} = 100k$	100k	95k	105k	105k	95k	100k
$R_{bias2} = 100k$	100k	105k	95k	95k	105k	95k
$R_L = 100k$	95k	100k	95k	100k	105k	95k

Results – Low Noise Amplifier @ 10GHz

Results of some Injected Faults

Circuit Parameter	Coefficients out of bounds	Detected
R_{bias} down 25%	$a_0 - a_4$	Yes
L_C down 15%	a_2, a_5	Yes
C_{C1} up 10%	a_1, a_2, a_3	Yes
L_1 down 25%	$a_0 - a_4$	Yes
L_2 up 15%	a_0, a_4	Yes
L_f up 10%	a_1, a_2	Yes
C_f up 10%	a_4, a_5	Yes
C_{C2} down 10%	a_4, a_5	Yes

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Fault Diagnosis

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To determine the circuit parameters responsible for deviation of circuit from its desired behavior.

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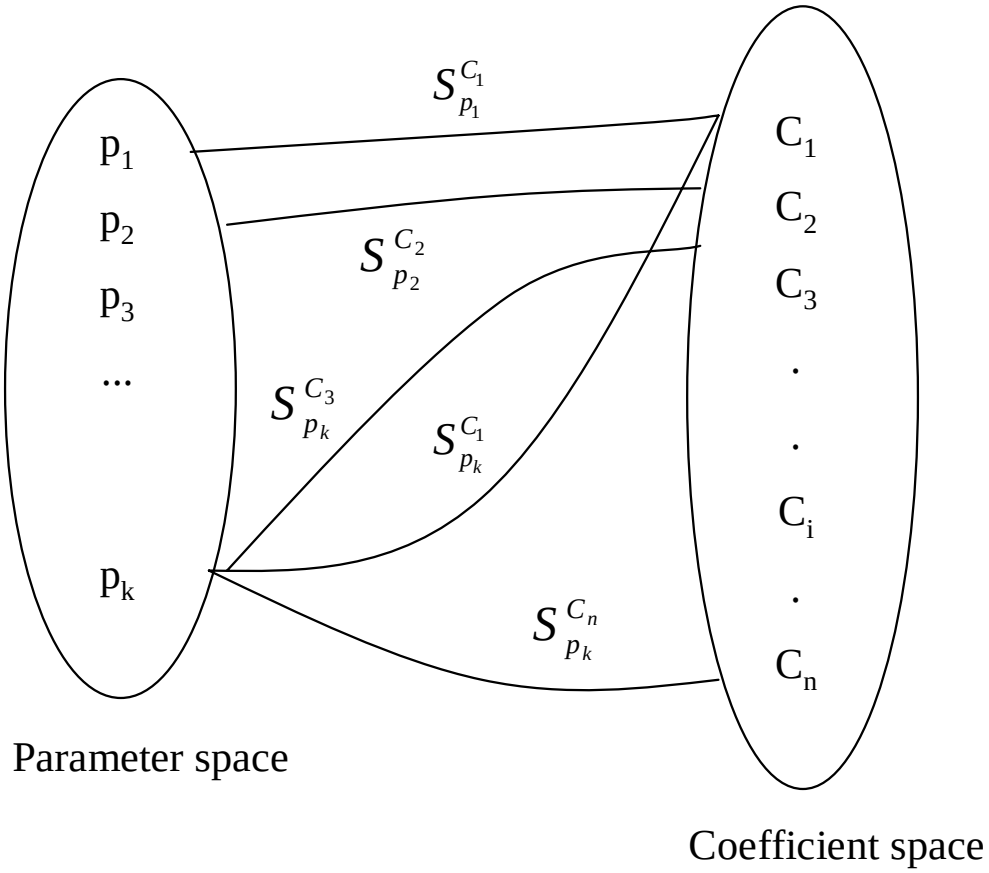
Sensitivity based diagnosis

$$S_{p_k}^{C_i} = \frac{p_k}{C_i} \frac{\partial C_i}{\partial p_k}$$

Fault Diagnosis



Possible relation between various parameters and coefficients

Results – Low Noise Amplifier

Fault Diagnosis at f = 10 GHz

Fault injected	Coefficient status	Diagnosed fault sites
R_{bias} down 25%	$a_0 - a_4$	R_{bias}
L_C down 15%	a_2, a_5	L_C or C_{C1}
C_{C1} up 10%	a_1, a_2, a_3	C_{C1} or L_C
L_1 down 25%	$a_0 - a_4$	L_1
L_2 up 15%	a_0, a_4	L_2
L_f up 10%	a_1, a_2	L_f or C_f
C_f up 10%	a_4, a_5	L_f
C_{C2} down 10%	a_4, a_5	C_{C2}

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Conclusions and Future Work

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- Technique for parametric fault detection in analog circuits – faults as small as 10% were uncovered for LNA example
- Diagnosis based on Sensitivity of Polynomial Coefficients to circuit parameters
- Limitation – Extensive fault simulations required to cover all corner cases

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In Future

- Neural models to map specifications to polynomial coefficients
- To implement proposed test scheme as BIST by storing polynomial coefficients on chip

Acknowledgments

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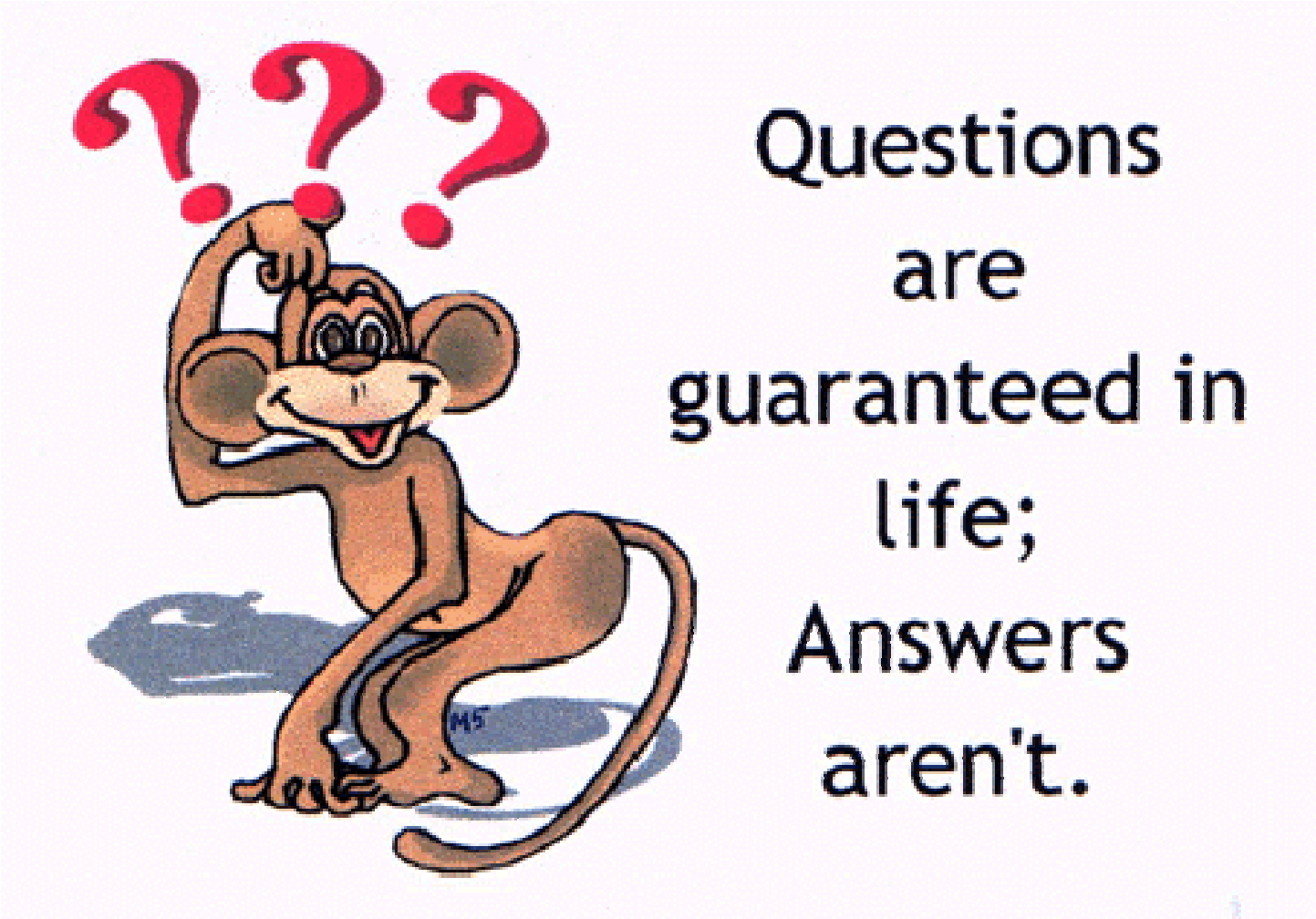
Thanks for your Attention!


Questions
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