Specification Test Minimization for Given Defect Level

Suraj Sindia* and Vishwani D. Agrawal
Department of Electrical and Computer Engineering
Auburn University, Auburn, AL 36849, USA
Email: szs0063@auburn.edu, vagrawal@eng.auburn.edu

***Abstract*—An accepted industry practice for testing of analog and RF circuits is to use specification-based tests. These tests are capable of providing a very low defect level but tend to be long and costly. In this work, we focus on minimizing the specification-based tests without exceeding any given defect level. We use Monte Carlo simulation to determine the probabilities with which a test covers specifications it was not originally intended to cover. These probabilities and the given defect level then define an integer linear programming (ILP) model for eliminating unnecessary tests. This paper gives sufficient evidence of successful implementation of the proposed methodology. A hypothetical example of ten specifications illustrates that depending upon the defect level requirement up to half of the tests may be eliminated. Monte Carlo simulation using spice for probabilistic characterization of tests versus specifications of a commercially available operational amplifier circuit is presented as evidence for the applicability of the technique.**

***Keywords:* Analog and mixed-signal testing, defect-level, RF testing, specification-based testing, test optimization.**

I. Introduction

A. Test Cost and Defect Level

Testing an integrated circuit chip more than what is necessary adds to the cost of testing and, consequently, increases the total cost of shipping the chip. The minimum amount of testing to be done on a chip is determined by the tolerable *defect level*. Defect level is the fraction of bad devices passing the test [9].

B. Rising Specification Test Cost of Analog Circuits

Classifying analog, mixed-signal, and radio-frequency circuits as "good" or "bad" requires them to be tested against a set of specifications that the circuits are designed for. These specifications usually have a nominal value bounded within a continuous range of minimum and maximum values. Tests, henceforth referred to as specification tests, often require expensive test instruments and complex test setups [8], [11] depending on the specification and the circuit that is being tested. At modern technology nodes, testing analog and RF circuits against all their specifications is becoming expensive and costs as much as manufacturing the integrated circuit as shown by an international technology road map for semiconductors (ITRS) prediction [1] in Figure 1.

*Present address: Intel Corporation, Hillsboro, OR 97124, USA.

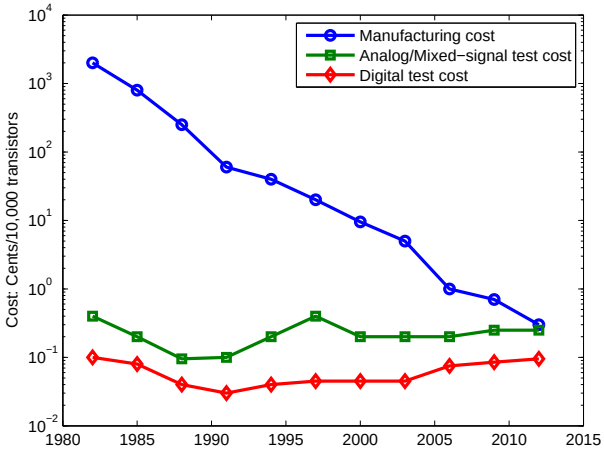

Fig. 1. Manufacturing cost per transistor has steadily declined over the years, whereas test cost per transistor has remained fairly steady over the years and is expected to remain so, catching up with manufacturing cost by 2015 or so per the ITRS prediction [1].

C. Contributions of This Paper

This paper provides a framework to reduce the testing cost by compacting specification test set. In order to do this, we leverage the inherent correlation that exists among specifications of a circuit. The correlations among circuit specifications allow us to define an integer linear program that minimizes the final test set while ensuring that the defect level does not exceed a desired threshold. Existing correlations among specifications of the circuit are estimated through Monte-Carlo simulation, which is done off line and only once before the start of the actual manufacturing test.

The rest of the paper is organized as follows. Section II formally states the problem. Section III elucidates the problem through a graphical representation. Section IV formulates an integer linear program that yields the optimized test set given a defect level threshold and cross-correlation among specification tests. A numerical example is solved to illustrate the methodology and the potential savings that can be achieved in Section V. Section VI describes an operational amplifier circuit example for which cross correlation among specification tests is estimated through Monte-Carlo simulation and an optimized test set is arrived at using the framework proposed in this paper. We conclude in Section VII.

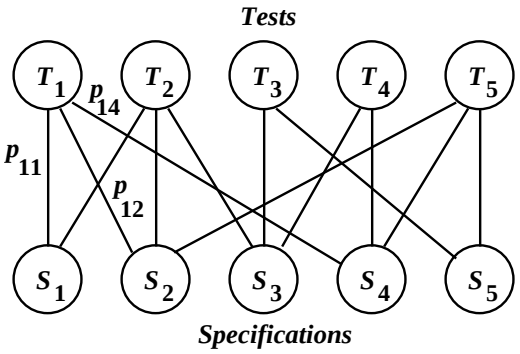

Fig. 2. Bipartite graph [6] of tests $\{T_i\}$ and specifications $\{S_i\}$ of a circuit under test (CUT). The edge label p_{ij} is the probability of testing specification S_j by test T_i.

II. Problem Statement

Consider a circuit under test (CUT) that has specifications $S_1, S_2, \cdots S_k$. A test T_i is used to check the correctness of specification S_i. We assume that these k tests are "perfect"; ith test will detect any out of range deviation of the ith specification. Such tests are often derived and used in practice because they guarantee a "zero" (assumed perfect) defect-level. Defect-level refers to test escapes or faulty devices passing test [9] and it is often measured in parts per million (PPM).

The specification-based test is very thorough (almost zero defect-level) but it can be very long. Typically, it requires long test time on the automatic test equipment (ATE), making the test expensive. A significant problem in the industry is to reduce the cost of testing without raising the defect level. In this work we propose an optimization solution.

In general, for k specifications the number of tests may or may not be exactly k. But, that does not affect the way the following analysis is done.

III. A Graph Representation

Figure 2 shows a bipartite graph [6] with two sets of vertices, tests and specifications. In the graph an edge label p_{ij} represents the probability of test T_i testing specification S_j. In general, the test T_i is designed to test for specification S_i. Therefore, we assume $p_{ii} = 1.0$ for all i. For edges for which $i \neq j$ we find the probabilities p_{ij} by Monte Carlo simulation as described in Section VI. Note that, in general, $p_{ij} \neq p_{ji}$. Also, a specification may be testable only by a subset of tests. That accounts for the missing edges in the graph for which the label $p_{ij} = 0$.

IV. An Integer Linear Program

We define a [0,1] integer variable x_i for each test T_i. We will formulate an integer linear program (ILP) to determine the values $\{x_i\}$ such that if $x_i = 1$, test T_i will be retained and if $x_i = 0$, T_i will be discarded. Thus, the objective function for the ILP is,

$$\text{minimize} \sum_{i=1}^{k} x_i \tag{1}$$

Next, we derive a set of linear constraints. Suppose, we wish the defect-level not to exceed a given value dl. We define the probability $P(S_j)$ of covering (fully testing) the specification S_j. Then,

$$1 - \prod_{j=1}^{k} P(S_j) \leq dl \tag{2}$$

If we assign equal significance to all specifications, then each specification should equally contribute to the defect-level. Thus,

$$(1 - dl)^{1/k} \leq P(S_j), \forall j \tag{3}$$

which can also be expressed as,

$$1 - P(S_j) \leq 1 - (1 - dl)^{1/k}, \forall j \tag{4}$$

Since a specification may be covered by multiple tests, we determine its coverage probability as,

$$P(S_j) = 1 - \prod_{i=1}^{k} (1 - p_{ij})^{x_i} \tag{5}$$

When $x_i = 1$, i.e., test T_i is retained, it contributes a factor $(1 - p_{ij})$ to the product in equation (5), and when $x_i = 0$, i.e., T_i is discarded, it contributes 1 to the product. We can also write,

$$\ln[1 - P(S_j)] = \sum_{i=1}^{k} x_i \ln(1 - p_{ij}) \tag{6}$$

From equations (4) and (6), we get the linear constraints for the ILP:

$$\sum_{i=1}^{k} x_i \ln(1 - p_{ij}) \leq \ln[1 - (1 - dl)^{1/k}], \ j = 1, \ 2, \cdots k \tag{7}$$

TABLE I
TEST COVERAGE PROBABILITIES (p_{ij}) IN A HYPOTHETICAL EXAMPLE WITH 10 SPECIFICATIONS AND 10 TESTS.

Specification	p_{ij} values for tests									
	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9	T_{10}
S_1	1.00	0.97	0.94	0.91	0.88	0.85	0.82	0.79	0.76	0.73
S_2	0.73	1.00	0.97	0.94	0.91	0.88	0.85	0.82	0.79	0.76
S_3	0.76	0.73	1.00	0.97	0.94	0.91	0.88	0.85	0.82	0.79
S_4	0.79	0.76	0.73	1.00	0.97	0.94	0.91	0.88	0.85	0.82
S_5	0.82	0.79	0.76	0.73	1.00	0.97	0.94	0.91	0.88	0.85
S_6	0.85	0.82	0.79	0.76	0.73	1.00	0.27	0.26	0.17	0.03
S_7	0.88	0.85	0.82	0.79	0.76	0.15	1.00	0.36	0.30	0.04
S_8	0.91	0.88	0.85	0.82	0.79	0.02	0.41	1.00	0.37	0.04
S_9	0.94	0.91	0.88	0.85	0.82	0.25	0.17	0.39	1.00	0.40
S_{10}	0.97	0.94	0.91	0.88	0.85	0.38	0.15	0.14	0.06	1.00

TABLE II
ILP OPTIMIZATION IN 10-TEST HYPOTHETICAL EXAMPLE.

Defect level	ILP result: $x_i = 1$, T_i selected, else discarded										Number of	**Test size**
dl in PPM	x_1	x_2	x_3	x_4	x_5	x_6	x_7	x_8	x_9	x_{10}	selected tests	**reduction (%)**
1	1	0	1	1	0	1	1	1	1	1	8	**20**
10	0	1	0	1	0	1	1	1	1	1	7	**30**
100	1	1	0	0	0	1	1	1	1	1	7	**30**
1,000	1	0	0	0	0	1	1	1	1	1	6	**40**
10,000	1	1	1	1	1	0	0	0	0	0	5	**50**

V. A HYPOTHETICAL EXAMPLE

Consider ten specifications, $S_1, \cdots S_{10}$, and their respective tests, $T_1, \cdots T_{10}$. Probabilities of each test covering various specifications are summarized in Table I. We have skewed the test coverage probabilities to demonstrate the compaction of tests as the defect level is varied, but such high cross correlation in analog circuit specification tests is not uncommon and has been reported in the literature [10]. For an illustration, we assume a defect level 1,000 parts per million (PPM), i.e., $dl = 10^{-3}$.

For minimizing the tests we use the integer linear programming formulation of Section IV. The objective function (1) is:

$$\text{minimize} \sum_{i=1}^{10} x_i, \tag{8}$$

Subject to the set of constraints (7). Right hand side of inequality (7) is evaluated as, $\ln[1-(1-10^{-3})^{1/10}] = -9.21$. To avoid $\ln 0 = -\infty$ coefficients on the left hand side, we approximate probabilities like $p_{ii} = 1.0 \approx 1 - 10^{-15}$. Therefore, the corresponding coefficient evaluates to $\ln(10^{-15}) = -34.54$:

$$\{x_i\} = integer[0,1], 1 \leq i \leq 10$$

$$-34.54x_1 - 3.51x_2 - 2.81x_3 - 2.41x_4 - 2.12x_5 - 1.90x_6 - 1.71x_7 - 1.56x_8 - 1.43x_9 - 1.31x_{10} \leq -9.21,$$
$$-1.31x_1 - 34.54x_2 - 3.51x_3 - 2.81x_4 - 2.41x_5 - 2.12x_6 - 1.90x_7 - 1.71x_8 - 1.56x_9 - 1.43x_{10} \leq -9.21,$$
$$-1.43x_1 - 1.31x_2 - 34.54x_3 - 3.51x_4 - 2.81x_5 - 2.41x_6 - 2.12x_7 - 1.90x_8 - 1.71x_9 - 1.56x_{10} \leq -9.21,$$
$$-1.56x_1 - 1.43x_2 - 1.31x_3 - 34.54x_4 - 3.51x_5 - 2.81x_6 - 2.41x_7 - 2.12x_8 - 1.90x_9 - 1.71x_{10} \leq -9.21,$$
$$-1.71x_1 - 1.56x_2 - 1.43x_3 - 1.31x_4 - 34.54x_5 - 3.51x_6 - 2.81x_7 - 2.41x_8 - 2.12x_9 - 1.90x_{10} \leq -9.21,$$
$$-1.90x_1 - 1.71x_2 - 1.56x_3 - 1.43x_4 - 1.31x_5 - 34.54x_6 - 0.31x_7 - 0.30x_8 - 0.19x_9 - 0.03x_{10} \leq -9.21,$$
$$-2.12x_1 - 1.90x_2 - 1.71x_3 - 1.56x_4 - 1.43x_5 - 0.16x_6 - 34.54x_7 - 0.45x_8 - 0.36x_9 - 0.04x_{10} \leq -9.21,$$
$$-2.41x_1 - 2.12x_2 - 1.90x_3 - 1.71x_4 - 1.56x_5 - 0.02x_6 - 0.53x_7 - 34.54x_8 - 0.46x_9 - 0.04x_{10} \leq -9.21,$$
$$-2.81x_1 - 2.41x_2 - 2.12x_3 - 1.90x_4 - 1.71x_5 - 0.29x_6 - 0.19x_7 - 0.49x_8 - 34.54x_9 - 0.51x_{10} \leq -9.21,$$
$$-3.51x_1 - 2.81x_2 - 2.41x_3 - 2.12x_4 - 1.90x_5 - 0.48x_6 - 0.16x_7 - 0.15x_8 - 0.06x_9 - 34.54x_{10} \leq -9.21.$$

Solving this ILP using an open source solver [2] results in a minimized test set of only *six* tests by eliminating four tests, namely: T_1, T_2, T_3 and T_5, from the original test set of ten tests, T_1 through T_{10}.

Table II summarizes the optimized tests for various defect level values in the range 1 PPM through 10,000 PPM using

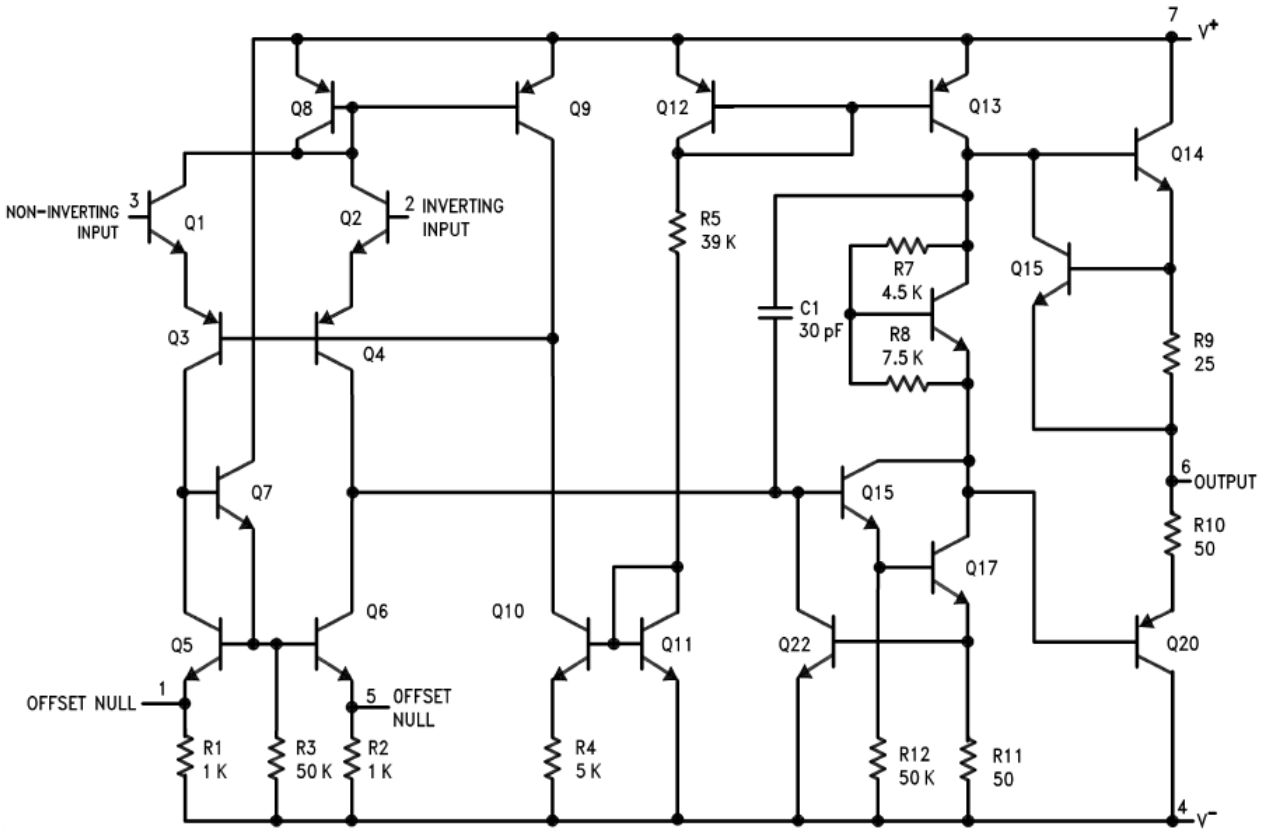

Fig. 3. Circuit schematic of operational amplifier LM741 [4] with nominal values of the components. This is the circuit example used for estimating correlation among specifications through Monte-Carlo simulation.

the ILP formulation laid out in Section IV for the test coverage probabilities of different specifications chosen in Table I. As can be seen in the table, test size reduction of 40% is achieved at a defect level of 1,000 PPM, which is a typical test escape accepted in custom analog circuits in deep sub-micron technology nodes such as 180nm or lower [7]. As one would expect, the test set size reduction varies directly as the defect level is allowed to increase. For example 20% reduction at $dl = 10$ PPM, whereas it is 50% at $dl = 10,000$ PPM. The potential test reduction could be higher if there is higher cross-correlation between circuit specifications, or if a higher defect level can be tolerated, or both.

In Table II we notice that even for 1 PPM, which represents a very high quality level, two tests have been eliminated. This is quite a normal occurrence considering the fact that each test may have targeted a separate specification.

VI. Case Study: Monte Carlo Simulation for p_{ij}

In order to obtain more realistic values of test coverage probabilities of specifications for any given analog circuit, we propose the use of Monte-Carlo simulation of the circuit using the simulation program with integrated circuit emphasis (SPICE) [3]. Here we intend to demonstrate the test minimization procedure illustrated in Section V on a commercially available operational amplifier tested across seven specifications, namely:

- S_1: DC gain
- S_2: Slew rate
- S_3: 3-dB bandwidth
- S_4: Input referred offset voltage
- S_5: Power supply rejection ratio
- S_6: Common mode rejection ratio
- S_7: Input bias current

A. Circuit Details

The operational amplifier circuit used for simulation with nominal values of the components is shown in the circuit diagram of Figure 3. This operational amplifier circuit is a simplified schematic of the Texas Instruments (TI) LM741 provided in its data-sheet [4]. The circuit has 22 active devices (bipolar junction transistors (BJT)), 12 resistors, and one capacitor. Five thousand instances of the circuit are created by sampling passive component (resistor and capacitor) values from a normal distribution, with the mean value of each component set to its nominal value (shown alongside the component in Figure 3) and standard deviation set to 5% of the mean value. For the active components in the circuit (NPN

TABLE III
OPERATIONAL AMPLIFIER SPECIFICATIONS FROM LM 741 DATA-SHEET [4] USED IN THIS CASE STUDY.

Specification		Values			Unit
Label	Description	Minimum	Nominal	Maximum	
S_1	Dc gain	50	200		V/mV
S_2	Slew rate	0.3	0.5		V/μs
S_3	3-dB bandwidth	0.4	1.5		MHz
S_4	Input referred offset voltage		$\pm$10	$\pm$15	mV
S_5	Power supply rejection ratio	86	96		dB
S_6	Common mode rejection ratio	80	95		dB
S_7	Input bias current		30	80	nA

and PNP BJT), β or dc current gain is sampled from a normal distribution with mean set to its nominal value of 625 and standard deviation set to 10% of its nominal value or 62.5. All other parameters of the BJT are left unchanged from their nominal values as specified in the model file [5].

B. Calculating p_{ij}

Table III lists the minimum, nominal, and maximum values of specifications S_1 through S_7 as given in the TI LM 741 data-sheet [4]. A circuit instance is considered to "fail" a given specification if the specification value (for that circuit instance) lies outside the minimum-maximum range of that specification. Note that some specifications are "single-ended," that is, they may not have either the minimum or the maximum bound; in such cases, the circuit instance is labeled as "fail" if it lies outside the permissible "single-ended" range.

We calculate the conditional test coverage of specification S_j by S_i, or in other words, the likelihood of test T_i for S_i covering S_j as follows:

$$p_{ij} = \frac{\text{Number of instances failing both } S_i \text{ and } S_j}{\text{Number of instances failing } S_j} \quad (9)$$

For the operational amplifier circuit LM 741 shown in Figure 3 all seven specifications S_1 through S_7 for the 5,000 circuit instances generated (as described in Section VI-A) are first measured. Next, the conditional test coverage between all pairs of specifications is obtained using equation (9). For example, out of the 5,000 circuit instances S_1 is violated by 45 circuit instances while S_2 is violated by 81 instances as shown in the graph of Figure 4. Seventeen circuit instances fail both S_1 and S_2 (labeled on the edge connecting nodes S_1 and S_2 in the graph.) This gives probability p_{12}, which is the probability of test for specification S_1 (i.e., T_1) covering specification S_2, $p_{12} = \frac{17}{81} = 0.21$. Similarly, p_{21}, which is the probability of test for specification S_2 (i.e., T_2) covering specification S_1, $p_{21} = \frac{17}{45} = 0.38$. Values of p_{ij} for the LM 741 circuit example across all seven specifications are listed in Table IV, where for the sake of clarity T_i is used as column header to signify the test for specification S_i.

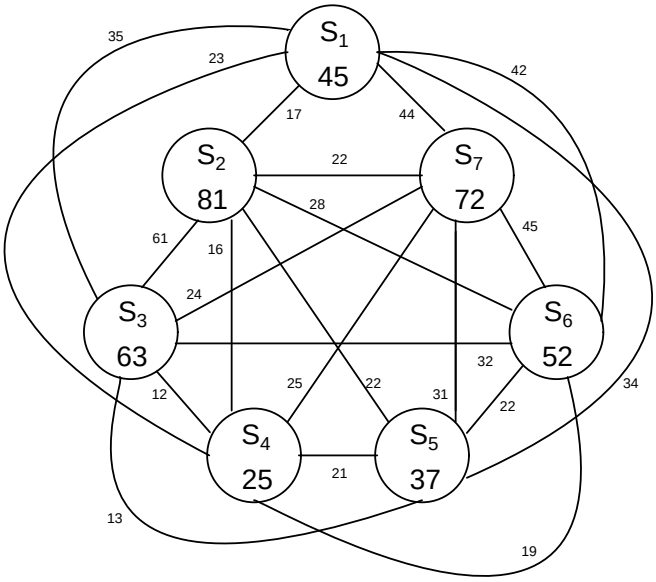

Fig. 4. A graph depicting the number of circuit instances failing each specification (noted inside the node) and the number of circuit instances failing both specifications (noted on the edges).

Next, we examine the specification test compression achievable for the LM 741 opamp using the integer linear program of Sections IV and V.

C. Results of Compaction and Discussion

Choosing a desired defect level dl anywhere in the range 1 to 100 PPM, the ILP reduces the number of specifications to be tested by one, from 7 to 6, by eliminating test T_4 for specification S_4. It is also intuitively clear why this may be so from Table IV as test T_7 covers S_4 with probability 1. Upon relaxing defect level, dl, further to 1,000 PPM, the number of specifications to be tested is reduced by one more specification by eliminating test T_1 for specification S_1 thereby giving a compacted set of 5 tests. Defect level

TABLE IV
PROBABILITIES p_{ij} FOR OPAMP LM 741 EXAMPLE.

Specification	p_{ij} values for tests						
	T_1	T_2	T_3	T_4	T_5	T_6	T_7
S_1	1.00	0.38	0.78	0.51	0.76	0.93	0.98
S_2	0.21	1.00	0.75	0.20	0.27	0.35	0.27
S_3	0.56	0.97	1.00	0.19	0.21	0.51	0.38
S_4	0.92	0.64	0.48	1.00	0.84	0.76	1.00
S_5	0.92	0.59	0.35	0.57	1.00	0.59	0.84
S_6	0.81	0.54	0.62	0.37	0.42	1.00	0.87
S_7	0.61	0.31	0.33	0.35	0.43	0.62	1.00

10,000 PPM allows elimination of T_3 leaving only four tests. Further test compaction could be possible by varying the minimum/maximum thresholds used for the specifications. This line of research is currently being pursued.

VII. CONCLUSION

Considering that there is a pressing need to reduce test costs of analog, RF and mixed signal circuits we can reduce the test cost by leveraging the cross-correlation that exists among circuit specifications. An integer linear program optimally minimizes the test set while ensuring that the quality of the tested circuit does not degrade beyond a given threshold defect level. An illustrative example shows test size reduction of 40% at defect level of 1,000 PPM. Even more test reduction is possible if there is better correlation among circuit specifications, or if a higher defect level can be tolerated.

In Section IV, the objective function of equation (1) gives equal weight to all tests. In reality, however, different tests may have different complexities and they may require different application times. The test application time of test T_i can be used as a weight factor w_i to redefine the objective function as,

$$\text{minimize} \sum_{i=1}^{k} w_i x_i \tag{10}$$

While deriving equation (3) we made a simplifying assumption that each of the k specifications was equally significant. We thus distributed the defect level (dl) equally over all specifications, which allowed us to derive the linear constraints of equation 7. Lifting this assumption, i.e., treating some specifications as more critical than others, will require reformulation of the ILP model.

Any test minimization that preserves the defect level can, in general, reduce the diagnostic capability of tests. In high-volume production testing, test time reduction is usually a priority. In characterization testing, such as during the initial yield ramp up, diagnosis is important. An alternative criterion for test optimization might be to preserve or maximize the diagnostic resolution instead of defect level. Our future research will focus on diagnostic tests as well. The ILP formulation described in this paper can also be used for minimizing alternate tests [12] for a given circuit, much like minimizing conventional specification tests demonstrated here.

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