

High Sensitivity Test Signatures for Unconventional Analog Circuit Test Paradigms

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Abstract—A method of testing for parametric faults in analog circuits based on a polynomial representation of fault-free function of the circuit is presented. The response of the circuit under test (CUT) is estimated as a polynomial in the root mean square (RMS) magnitude of the applied input voltage at a relevant frequency or DC. The test then classifies the CUT as fault-free or faulty based upon a comparison of the estimated polynomial coefficients with those of the fault-free circuit. The test application needs very little augmentation of the circuit to make it testable as only output parameters are used for classification. The method is validated on an active elliptic filter and is shown to uncover parametric faults causing deviations as small as 5% from nominal values. Fault diagnosis based upon sensitivity of polynomial coefficients at relevant frequencies is discussed. Another type of circuit signatures in the form of probability moments of the output when test input is random noise are also proposed. It is shown that the sensitivity of either signature can be enhanced by a newly proposed nonlinear V-transform. Finally, an adaptive test framework leveraging from these signatures and the transform technique is shown to improve defect level and yield loss.

I. INTRODUCTION

Testing of linear circuits is well studied and several methods can be found in the literature [9], [15]–[17]. Guo and Savir [9] describe a scheme that is representative of coefficient based test schemes for analog circuits. The circuit under test (CUT) is subjected to frequency rich input signals and the output voltage alone is observed. With these input-output pairs one can estimate transfer function coefficients of the CUT under the assumption that it is a linear time-invariant (LTI) system. Next they compare these transfer function coefficient estimates with the ideal circuit transfer function coefficients, which are known a priori. The CUT is classified faulty if any of the estimated coefficients is outside a tolerance range. For example, the circuit shown in Figure 1 is a second order low pass filter and has a transfer function:

$$H(s) = \frac{1}{(R_1 R_2 C_1 C_2) s^2 + (R_1 C_1 + (R_1 + R_2) C_2) s + 1} \quad (1)$$

Clearly, the coefficients of the transfer function, $b_0 = 1$, $b_1 = (R_1 C_1 + (R_1 + R_2) C_2)$, $b_2 = R_1 R_2 C_1 C_2$, are functions of circuit parameters R_1 , R_2 , C_1 , C_2 . Assuming single parametric faults, they find the minimum drift in any of the circuit component values that will cause the coefficients b_1 or b_2 (b_0 here is a constant) to drift outside a tolerance range.

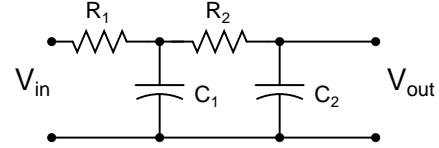


Fig. 1. Second order low pass filter.

However, this method [9] *necessarily needs the CUT to be linear*, as a frequency domain transfer function is possible only for an LTI system.

Several methods have been proposed for parametric fault testing of non-linear circuits [1], [2], [4]–[8], [13], [20]. To address the issue of parametric deviation, we would typically need more observables to have an idea about the parametric drift in circuit parameters. This would mean an increase in the complexity of the sensing circuit. However, we would also want minimal augmentation to tap any of the internal circuit nodes or currents. To overcome these seemingly contrasting requirements the method intended should have some way of “seeing through” the circuit with only the outputs and inputs at its disposal. References [9], [17] give such strategies for linear circuits as described earlier.

To extend this idea to general non-linear circuits we adopt a strategy where we express the function of the circuit as a polynomial using a Taylor series expansion [12] in terms of input voltage v_{in} , about the point $v_{in} = 0$ as follows:

$$v_{out} = f(v_{in}) = f(0) + \frac{f'(0)}{1!} v_{in} + \frac{f''(0)}{2!} v_{in}^2 + \frac{f'''(0)}{3!} v_{in}^3 + \dots + \frac{f^{(n)}(0)}{n!} v_{in}^n + \dots \quad (2)$$

where $f(x)$ is a real function of x .

This method is very general as any analog circuit can be tested using this model. The technique applies equally well to linear circuits, which are a subclass of the general non-linear circuits considered in this paper (originally appearing in [30], [31]). The accuracy, resolution and observability of faults uncovered depends on the degree of the polynomial expansion used in practice. Ignoring the higher order terms in (2), we can expand v_{out} up to some n th power of v_{in} , which gives us the approximation in (3). In order to increase the available observables to better track down parametric faults

we can expand v_{out} at multiple frequencies. Thus, we will have $m \times (n+1)$ observables where m is the number of tones (frequencies) including DC at which v_{out} is expanded and n is the degree of expansion [10]:

$$v_{out} = a_0 + a_1 v_{in} + a_2 v_{in}^2 + \dots + a_n v_{in}^n \quad (3)$$

where $a_0, a_1, a_2, \dots, a_n$ are all real functions of circuit parameters $p_k \forall k$.

The special case of DC test that detects a subset of faults, was given in a recent paper [30]. Further, we assume that normal parameter variations (normal drift) in a good circuit are within a fraction α of their nominal value, where $\alpha \ll 1$. That is, every parameter p_k is allowed to vary within the hypercube $p_{k,nom}(1 - \alpha) < p_k < p_{k,nom}(1 + \alpha) \forall k$, where $p_{k,nom}$ is the nominal value of parameter p_k . Whenever one or more coefficient values slip outside this hypercube we get a different set of coefficients reflecting a detectable fault. Therefore, equation (4) describes the hypercube for all parameters that correspond to either good machine values or undetectable parametric faults [4], [9], [20]:

$$a_{i,min} < a_i < a_{i,max} \quad \forall i, \quad 0 \leq i \leq n \quad (4)$$

This paper is organized as follows. Section II analyzes the coefficients of the polynomial expansion of the function $f(v_{in})$ and determines the detectable fault sizes of parameters. In Section III, we illustrate the testing problem being solved and discuss the proposed solution with an example. In Section IV, we generalize the solution to an arbitrarily large circuit. Section V presents the simulation results for some standard circuits. Section VI outlines the method of fault diagnosis using the proposed method. Sections VII and VIII introduce another type of signature, namely, probability moments and sensitivity enhancement of signatures by V-transform, respectively, that are described in detail elsewhere [24], [27]. An adaptive framework that leverages on the proposed circuit signatures is discussed in IX. We conclude in Section X.

The material presented in the paper is based on the doctoral dissertation [21] of the first author, written under the guidance of the second author. This manuscript is an entry to the final round of the *TTTC E. J. McCluskey Doctoral Thesis Contest* at 2013 International Test Conference.

II. PRELIMINARIES

The coefficients $a_i \forall i \ 0 \leq i \leq n$ are, in general, non-linear functions of circuit parameters $p_k \forall k$. The rationale behind using these coefficients as metrics in classifying CUT as faulty or fault-free is based on the dependence of the coefficients on circuit parameters.

A. Analysis of Polynomial Coefficients

We discuss several significant results, proofs of which can be found elsewhere [21].

Theorem 1. *If coefficient a_i is a monotonic function of all parameters, then a_i takes its limiting (maximum and minimum)*

values when at least one or more of the parameters are at the boundaries of their individual hypercube.

Lemma 1. *If coefficient a_i is a non-monotonic function of one or more circuit parameters p_i , then a_i can take its limiting values anywhere inside the hypercube enclosing the parameters.*

From Theorem 1 and Lemma 1 it is clear that by exhaustively searching the space in the hypercube of each parameter we can get the maximum and minimum values of the polynomial coefficient. Typically this can be formulated as a non-linear optimization problem to find the maximum and minimum values of coefficient with constraints on parameters allowing only a normal drift.

Theorem 2. *In polynomial expansion of non-linear analog circuit there exists at least one coefficient that is a monotonic function of all circuit parameters.*

From Lemma 1 and Theorem 2 we find that circuit parameter deviations have a bearing on coefficients and monotonically varying coefficients can be used to detect parametric faults of the circuit parameters.

Theorem 3. *A continuous non-monotonic function $f : \mathbb{R} \rightarrow \mathbb{R}$ can be decomposed into piecewise monotonic functions as follows:*

$$f(x) = f(x)u(x_0 - x) + f(x)(u(x - x_0) - u(x - x_1)) + f(x)(u(x - x_1) - u(x - x_2)) + \dots + f(x)(u(x - x_{n-1}) - u(x - x_n)) \quad (5)$$

where x_0, x_1, \dots, x_n are all stationary points of $f(x)$ and

$$u(x) = \begin{cases} 1 & \forall x \geq 0 \\ 0 & \forall x < 0 \end{cases}$$

Using Theorem 3, we can express every polynomial coefficient as a monotonic function of circuit parameters and thus we can use every coefficient to track the drifts in circuit parameters.

B. Definitions

Definition 1. *Minimum size detectable fault (MSDF), ρ , of a parameter is defined as the minimum fractional deviation of a circuit parameter from its nominal value for it to be detectable with all other parameters being held at their nominal values. The fractional deviation can be positive or negative and is named upside-MSDF (UMSDF) or downside-MSDF (DMSDF), accordingly.*

Definition 2. *Nearly-minimum size detectable fault (NMSDF), ρ^* , of a parameter is defined as some fractional deviation of the circuit parameter from its nominal value with all the other parameters being held at their nominal values that is close to its MSDF with an error, ϵ (infinitesimally small). That is,*

$$\epsilon = |\rho - \rho^*| \quad \epsilon \ll 1 \quad (6)$$

NMSDF also has notions of upside and downside as in the case of MSDF. In equation (6), ϵ can be perceived as a coefficient of uncertainty about the MSDF of a parameter. Let ψ be the set of all coefficient values spanned by the parameters while varying within their normal drifts, i.e.,

$$\psi = \{v_0, v_1, \dots, v_n \mid v_0 \in A_0, v_1 \in A_1, \dots, v_n \in A_n\} \\ \forall_k \quad p_{k,nom}(1 - \alpha) < p_k < p_{k,nom}(1 + \alpha)$$

Note that by Definitions 1 and 2, ψ includes all possible values of coefficients that are not detectable. Any parametric fault inducing coefficient value outside this set ψ will result in a detectable fault.

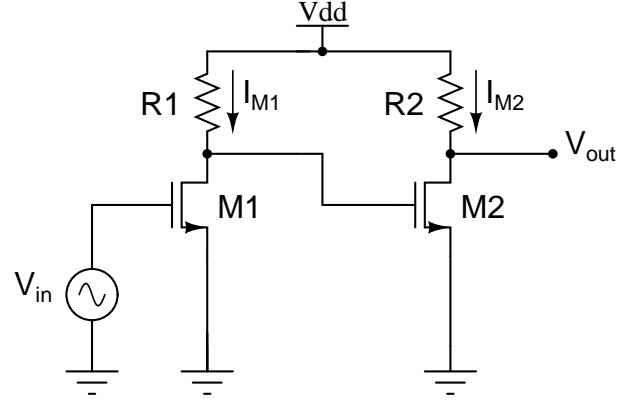


Fig. 2. Cascade amplifier.

III. PROBLEM DESCRIPTION AND SKETCH OF SOLUTION

We shall first give an illustrative example of calculation of limits for polynomial coefficients for a simple circuit using MOS transistors. We shall follow that up with MSDF values for the circuit parameters.

Example: Two stage amplifier. Consider the cascade amplifier shown in Figure 2. The output voltage V_{out} in terms of input voltage results in a fourth degree polynomial equation as follows:

$$v_{out} = a_0 + a_1 v_{in} + a_2 v_{in}^2 + a_3 v_{in}^3 + a_4 v_{in}^4 \quad (7)$$

where the constants a_0, a_1, a_2, a_3 are defined symbolically for transistors M1 and M2 operating in the saturation region:

$$a_0 = V_{DD} - R_2 K \left(\frac{W}{L}\right)_2 \left\{ \frac{(V_{DD} - V_T)^2 + R_1^2 K^2 \left(\frac{W}{L}\right)_1^2 V_T^4 - 2(V_{DD} - V_T) R_1 \left(\frac{W}{L}\right)_1 V_T^2}{2(V_{DD} - V_T) R_1 \left(\frac{W}{L}\right)_1 V_T^2} \right\}$$

$$a_1 = R_2 K \left(\frac{W}{L}\right)_2 \left\{ \frac{4R_1^2 K^2 \left(\frac{W}{L}\right)_1^2 V_T^3 + 2(V_{DD} - V_T) R_1 K \left(\frac{W}{L}\right)_1 V_T}{2(V_{DD} - V_T) R_1 \left(\frac{W}{L}\right)_1 V_T^2} \right\}$$

$$a_2 = R_2 K \left(\frac{W}{L}\right)_2 \left\{ \frac{2(V_{DD} - V_T) R_1 K \left(\frac{W}{L}\right)_1}{-6R_1^2 K^2 \left(\frac{W}{L}\right)_1^2 V_T^2} \right\}$$

$$a_3 = 4V_T K^3 \left(\frac{W}{L}\right)_1^2 \left(\frac{W}{L}\right)_2^2 R_1^2 R_2$$

$$a_4 = -K^3 \left(\frac{W}{L}\right)_1^2 \left(\frac{W}{L}\right)_2^2 R_1^2 R_2 \quad (8)$$

When we substitute the nominal values, $V_{DD} = 1.2V$, $V_T = 400mV$, $\left(\frac{W}{L}\right)_{M1} = \frac{1}{2} \left(\frac{W}{L}\right)_{M2} = 20$, and $K = 100\mu A/V^2$, we get the coefficients in terms of parameters R_1 and R_2 , as

follows:

$$a_0 = 1.2 - R_2 \begin{pmatrix} 2.56 \times 10^{-3} + 1.024 \times 10^{-7} R_1^2 \\ -5.12 \times 10^{-4} R_1 \end{pmatrix}$$

$$a_1 = 4.096 \times 10^{-9} R_1^2 R_2 + 5.12 \times 10^{-6} R_1 R_2$$

$$a_2 = 1.28 \times 10^{-5} R_1 R_2 - 1.536 \times 10^{-8} R_1^2 R_2 \quad (9)$$

$$a_3 = 2.56 \times 10^{-8} R_1^2 R_2$$

$$a_4 = 1.6 \times 10^{-8} R_1^2 R_2$$

To find the limiting values of the coefficient a_0 we assume the parameters R_1 and R_2 deviate by fractions x and y from their nominal values, respectively. For maximizing a_0 we have the objective function as given by (10), subject to constraints (11) through (15). Note that here we have set out to find MSDF of R_1 . Similar approach can be used to find the MSDF of R_2 .

$$1.2 - R_{2,nom}(1 + y) \left\{ \frac{2.56 \times 10^{-3} + 1.024 \times 10^{-7} R_{1,nom}^2 (1 + x)^2}{-5.12 \times 10^{-4} R_{1,nom} (1 + x)} \right\} \quad (10)$$

$$4.096 \times 10^{-9} R_{1,nom}^2 (1 + x)^2 R_{2,nom} (1 + y) + 5.12 \times 10^{-6} R_{1,nom} (1 + x) R_{2,nom} (1 + y) = 4.096 \times 10^{-9} R_{1,nom}^2 (1 + \rho)^2 R_{2,nom} + 5.12 \times 10^{-6} R_{1,nom} (1 + \rho) R_{2,nom} \quad (11)$$

$$1.28 \times 10^{-5} R_{1,nom} (1 + x) R_{2,nom} (1 + y) - 1.536 \times 10^{-8} R_{1,nom}^2 (1 + x)^2 R_{2,nom} (1 + y) = 1.28 \times 10^{-5} R_{1,nom} (1 + \rho) R_{2,nom} - 1.536 \times 10^{-8} R_{1,nom}^2 (1 + \rho)^2 R_{2,nom} \quad (12)$$

$$2.56 \times 10^{-8} R_{1,nom}^2 (1 + x)^2 R_{2,nom} (1 + y) = 2.56 \times 10^{-8} R_{1,nom}^2 (1 + \rho)^2 R_{2,nom} \quad (13)$$

$$1.6 \times 10^{-8} R_{1,nom}^2 (1 + x)^2 R_{2,nom} (1 + y) = 1.6 \times 10^{-8} R_{1,nom}^2 (1 + \rho)^2 R_{2,nom} \quad (14)$$

TABLE I
MSDF FOR CASCADE AMPLIFIER OF FIGURE 2 WITH $\alpha = 0.05$.

Circuit parameter	%upside MSDF	%downside MSDF
Resistor R_1	10.3	7.4
Resistor R_2	12.3	8.5

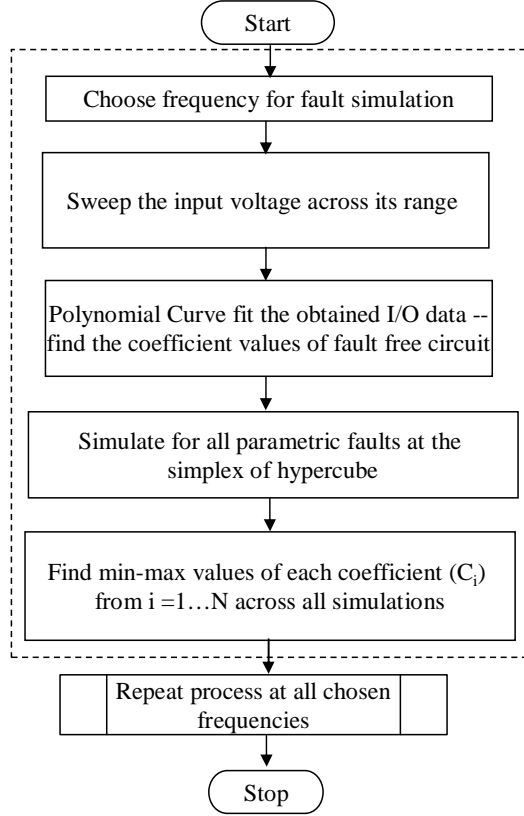


Fig. 3. Flow chart showing fault simulation process and bounding of coefficients.

$$-\alpha \leq x, y \leq \alpha \quad (15)$$

The extreme values for x and y on solving the above set of equations are obtained as, $x = -\alpha$ and $y = -\alpha$, giving us the MSDF value ρ for R_1 , as

$$\rho = (1 - \alpha)^{1.5} - 1 \approx 1.5\alpha - 0.375\alpha^2 \quad (16)$$

Table I gives the MSDF for R_1 and R_2 based on the above calculation.

IV. GENERALIZATION

In general, the calculation as described above cannot be done for an arbitrarily large circuit. Such circuits are handled by obtaining a nominal numeric polynomial expansion of the fault-free circuit. This is done by sweeping the input voltage across all possible values and noting the corresponding output voltages using any of the standard circuit simulators like SPICE [19]. Now, the output voltage is plotted against the input voltage. A polynomial is fitted to this curve and the

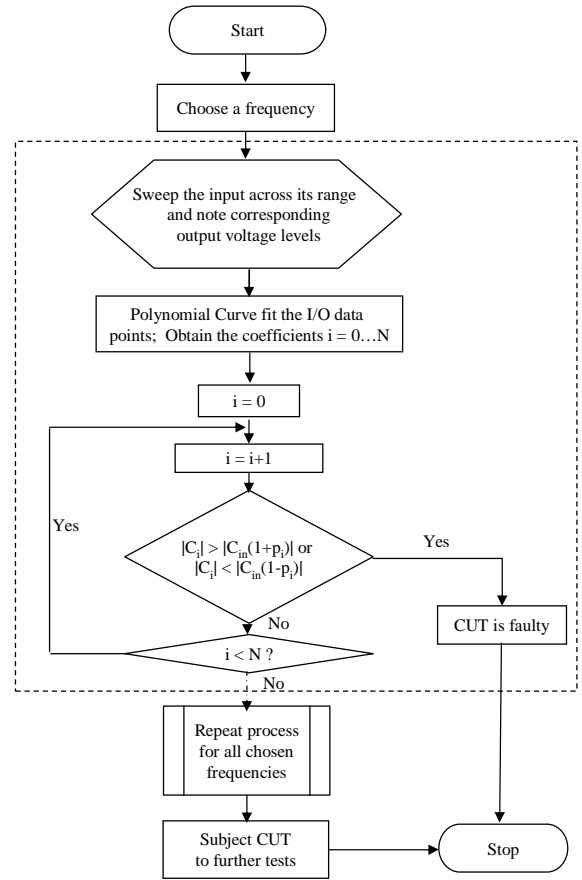


Fig. 4. Flow chart outlining test procedure for CUT.

coefficients of this polynomial are taken to be the nominal coefficients of the desired polynomial. The circuit is simulated for different drifts in the parameter values at equally spaced points from inside the hypercube enclosing each circuit parameter, spaced at a suitably chosen resolution ($=\epsilon$). Polynomial coefficients are obtained for each of these simulations. The maximum and the minimum values of a coefficient in this search are taken as the limiting values on that coefficient. This process of modeling the circuit as a polynomial expansion and obtaining limit values on coefficients is repeated at “key” frequencies of interest. For example, the cut-off frequency in case of a non-linear filter can be a good candidate for such characterization. Once the limit values on all coefficients have been determined the CUT is subjected to full range of input at DC and each of the “key” frequencies. Its response to input sweep is curve fitted to a polynomial of order same as the fault-free circuit. If there are any coefficients that lay outside the limit values of corresponding coefficients of the fault-free circuit, we can conclude the CUT is faulty. The converse is also true with a high probability that is inversely proportional to coefficient of uncertainty ϵ . Flow chart in Figure 3 summarizes the process of numerically finding the polynomial and finding the bounds on coefficients. Flow chart in Figure 4 outlines the procedure to test CUT using the described method.

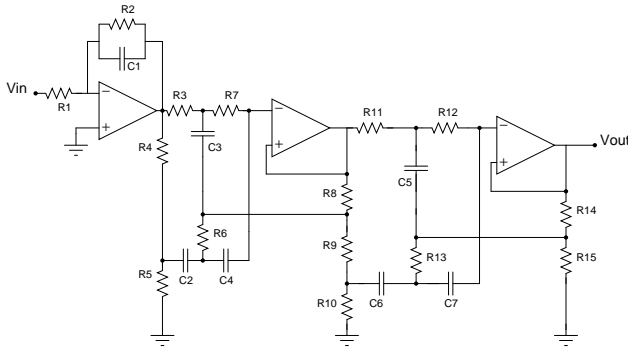


Fig. 5. Elliptic filter.

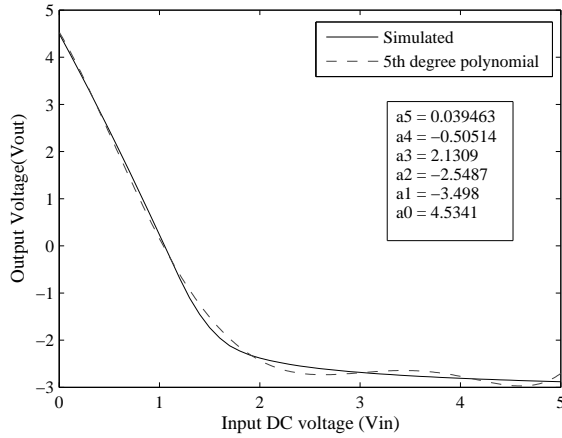


Fig. 6. DC response of elliptic filter with curve fitting polynomial.

V. EXPERIMENTAL RESULTS

We subjected an elliptic filter shown in Figure 5 to polynomial coefficient based test [29]. The circuit parameter values are as in the benchmark circuit maintained by Stroud et al. [11]. We simulated the circuit at four different frequencies. Two of them were chosen close to its 3dB cut-off frequency (f_c), which is 1000Hz. The estimated polynomial expansion obtained by curve fitting the I/O plots at DC and the frequencies $f=100\text{Hz}$, 900Hz , 1000Hz , 1100Hz are given by equations (17) through (21) and the corresponding plots tracing I/O response with polynomial are shown in Figures 6 through 10. The combinations of parameter values leading to limits on the coefficients for the tone at 1000Hz are shown in Table II. Further, the pass/fail detectability of several injected faults is tabulated in Table III.

$$v_{out} = 4.5341 - 3.498v_{in} - 2.5487v_{in}^2 + 2.1309v_{in}^3 - 0.50514v_{in}^4 + 0.039463v_{in}^5 \quad (17)$$

$$v_{out} = 3 + 7.9v_{in} - 11v_{in}^2 + 4.4v_{in}^3 - 0.78v_{in}^4 + 0.049v_{in}^5 \quad (18)$$

$$v_{out} = 2.5 + 5.4v_{in} - 8.6v_{in}^2 + 4v_{in}^3 - 0.77v_{in}^4 + 0.054v_{in}^5 \quad (19)$$

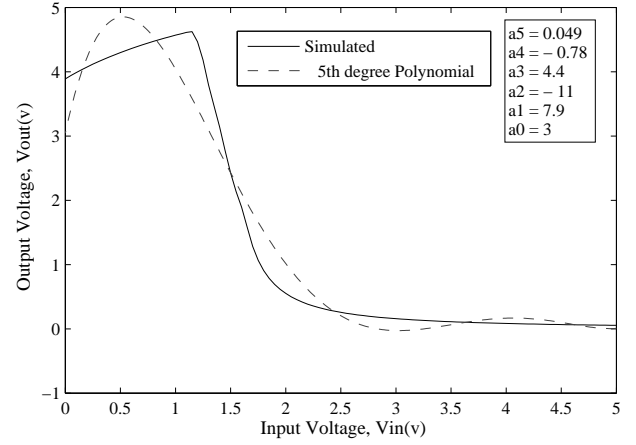


Fig. 7. Curve-fitting polynomial with coefficients at frequency = 100Hz.

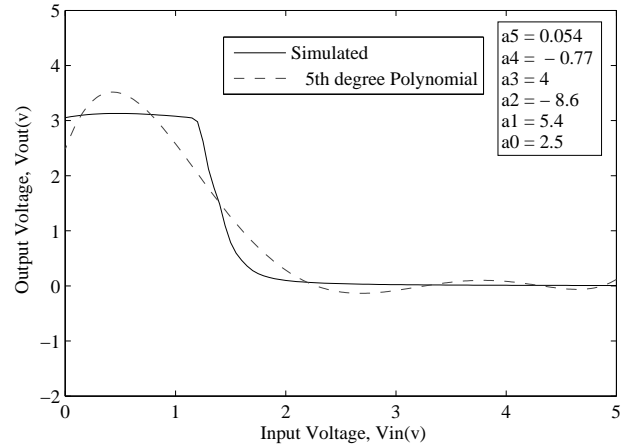


Fig. 8. Curve-fitting polynomial with coefficients at frequency = 900Hz.

$$v_{out} = 1.1707 + 2.4132v_{in} - 3.8777v_{in}^2 + 1.8035v_{in}^3 - 0.3465v_{in}^4 + 0.023962v_{in}^5 \quad (20)$$

$$v_{out} = 0.23 + 0.48v_{in} - 0.74v_{in}^2 + 0.34v_{in}^3 - 0.063v_{in}^4 + 0.0043v_{in}^5 \quad (21)$$

VI. FAULT DIAGNOSIS

Fault diagnosis using sensitivity of output to circuit parameters has been investigated in the literature [2], [34]. We have extended that approach exploiting the sensitivity of polynomial coefficients to circuit parameters [33]. The advantage of the new approach is an improved fault diagnosis without circuit augmentation. Sensitivity of i^{th} coefficient C_i to k^{th} parameter p_k is represented by $S_{p_k}^{C_i}$ and is given by:

$$S_{p_k}^{C_i} = \frac{p_k}{C_i} \frac{\partial C_i}{\partial p_k} \quad (22)$$

TABLE II
PARAMETER COMBINATIONS LEADING TO MAX AND MIN VALUES OF COEFFICIENTS WITH $\alpha = 0.05$ AT 1000Hz FOR ELLIPTIC FILTER.

Nominal Values	Circuit Parameters (Resistance in Ω , Capacitance in Farad)											
	Maximum values						Minimum values					
	a_0	a_1	a_2	a_3	a_4	a_5	a_0	a_1	a_2	a_3	a_4	a_5
$R_1 = 19.6k$	18.6k	18.6k	20.5k	20.5k	20.5k	18.6k	18.6k	18.6k	18.6k	18.6k	20.5k	20.5k
$R_2 = 196k$	205k	205k	205k	205k	186k	186k	205k	186k	186k	205k	205k	205k
$R_3 = 147k$	139k	139k	154k	139k	139k	139k	139k	139k	154k	139k	139k	139k
$R_4 = 1k$	950	950	1.05k	1.05k	1.05k	1.05k	1.05k	950	1.05k	950	950	1.05k
$R_5 = 71.5$	75	67	75	67	67	75	75	75	67	67	75	67
$R_6 = 37.4k$	35k	39k	39k	35k	35k	39k	39k	39k	35k	35k	35k	35k
$R_7 = 154k$	146k	146k	161k	161k	146k	146k	146k	146k	161k	161k	146k	146k
$R_8 = 260$	247	273	273	247	247	273	273	247	273	247	273	247
$R_9 = 740$	703	777	703	703	777	703	703	703	777	703	703	703
$R_{10} = 500$	475	525	525	475	525	525	475	525	475	525	525	475
$R_{11} = 110k$	115k	115k	115k	104k	104k	104k	115k	115k	104k	115k	104k	104k
$R_{12} = 110k$	104k	104k	115k	115k	115k	115k	115k	115k	104k	104k	115k	104k
$R_{13} = 27.4k$	28.7k	26k	26k	26k	28.7k	28.7k	26k	26k	28.7k	26k	28.7k	26k
$R_{14} = 40$	42	38	42	38	38	42	42	38	42	42	38	42
$R_{15} = 960$	912	912	912	912	912	1k	1k	1k	912	1k	912	912
$C_1 = 2.67n$	2.5n	2.5n	2.5n	2.5n	2.5n	2.5n	2.8n	2.5n	2.8n	2.8n	2.8n	2.5n
$C_2 = 2.67n$	2.5n	2.8n	2.8n	2.8n	2.5n	2.8n	2.8n	2.8n	2.8n	2.5n	2.8n	2.8n
$C_3 = 2.67n$	2.8n	2.8n	2.8n	2.5n	2.8n	2.8n	2.8n	2.8n	2.8n	2.5n	2.8n	2.8n
$C_4 = 2.67n$	2.5n	2.8n	2.5n	2.5n	2.5n	2.5n	2.5n	2.5n	2.8n	2.5n	2.5n	2.8n
$C_5 = 2.67n$	2.5n	2.5n	2.5n	2.5n	2.5n	2.8n	2.8n	2.8n	2.8n	2.8n	2.8n	2.8n
$C_6 = 2.67n$	2.5n	2.8n	2.5n	2.8n	2.5n	2.8n	2.8n	2.5n	2.8n	2.8n	2.8n	2.5n
$C_7 = 2.67n$	2.5n	2.8n	2.8n	2.8n	2.8n	2.5n	2.8n	2.5n	2.5n	2.5n	2.5n	2.8n

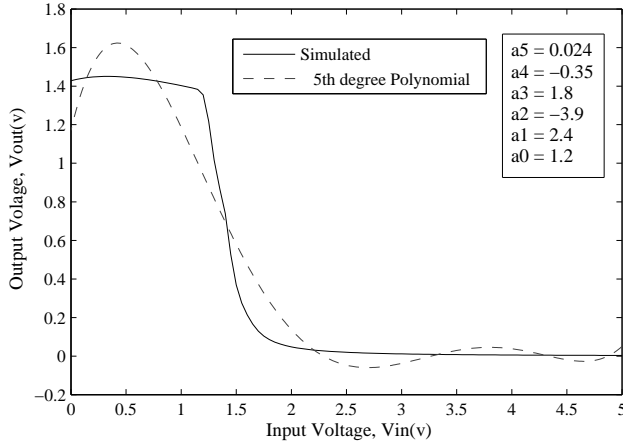


Fig. 9. Curve-fitting polynomial with coefficients at frequency = 1000Hz.

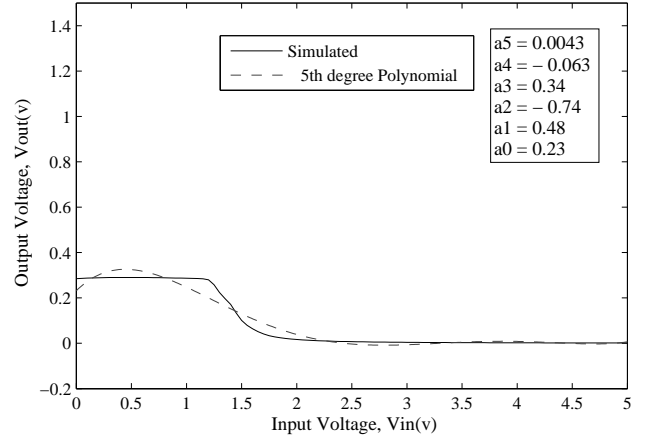


Fig. 10. Curve-fitting polynomial with coefficients at frequency = 1100Hz.

A. Computation of Sensitivities

Numerical computation of sensitivities given by (22) is accomplished by introducing fractional drifts ($= \alpha$) in each component ($p_k, \forall k$); simulating the circuit and measuring the fractional drift in each coefficient of the polynomial resulting from curve fitting operation. This way the numerical sensitivities are computed and a dictionary is maintained for sensitivities. The complexity in computation of sensitivities is linear in the number N of circuit parameters, i.e., $O(N)$.

B. Diagnosing Parametric Faults

Restricting ourselves to single parametric faults, we find the descending order of sensitivities of coefficients (with respect to circuit parameter) that have exceeded their limiting values.

The parameter with highest sensitivity is said to be at fault with a probability $P(\delta p_k | \delta C_i)$ (which can be interpreted as the confidence in diagnosing fault), given by (23):

$$P(\delta p_k | \delta C_i) = \phi \left(\frac{SC_{Pk}^i \delta p_k}{\delta C_i} \right), \quad (23)$$

where δp_k is the suspected drift in parameter p_k , δC_i is the measured drift in coefficient, and $\phi(\cdot)$ is an appropriately chosen function that normalizes its argument into a valid probability number (between 0 and 1) [18].

C. Fault Deduction

At each frequency, the above process of diagnosis is repeated. This gives the set of fault sites above a certain

TABLE III
DIAGNOSIS OF SOME INJECTED FAULTS IN ELLIPTIC FILTER AT VARIOUS FREQUENCIES.

Injected fault	Coefficients out of Bounds at					Detected
	DC	$f_1=100\text{Hz}$	$f_2=900\text{Hz}$	$f_3=1000\text{Hz}$	$f_4=1100\text{Hz}$	
R_1 down 15%	$a_0 - a_4$	$a_1 - a_4$	a_3, a_5	a_2, a_4	a_1, a_2	Yes
R_2 down 5%	a_2, a_5	a_1, a_3	a_1, a_5	a_1, a_2, a_5	a_1, a_2	Yes
R_3 up 10%	a_1, a_2, a_3	a_3, a_5	a_0, a_3, a_4	a_1, a_3, a_4	a_1, a_5	Yes
R_4 down 20%	$a_0 - a_3$	$a_1 - a_2$	a_2, a_3	a_1, a_2, a_3	a_2, a_3	Yes
R_5 up 15%	a_0, a_5	a_1	a_0, a_2	a_0, a_2, a_3	a_3	Yes
R_6 up 5%	—	a_1, a_2	a_2, a_3, a_5	a_1, a_3	a_1	Yes
R_7 down 10%	a_2, a_4	a_3, a_5	a_0, a_1, a_2	a_1, a_4, a_5	a_2, a_3	Yes
R_8 up 10%	—	a_2	a_0, a_4	a_0, a_2, a_5	a_3, a_4	Yes
R_9 down 5%	—	a_3, a_2	a_1, a_2, a_4	a_2, a_3, a_5	a_1, a_3	Yes
R_{10} up 15%	—	a_1, a_4	a_1, a_3, a_4	a_0, a_1, a_4	a_1, a_2	Yes
R_{11} down 10%	a_0, a_2	a_3, a_4	a_0, a_1	a_1, a_2, a_4	a_1, a_2	Yes
R_{12} down 15%	a_0, a_4	a_1, a_3	a_1, a_2, a_3	a_1, a_2	a_2, a_5	Yes
R_{13} up 5%	—	a_3, a_5	a_1, a_2	a_1, a_2, a_4	a_0, a_2	Yes
R_{14} up 20%	—	a_1, a_3	a_0, a_3, a_4	a_0, a_1, a_2	a_3, a_4	Yes
R_{15} up 5%	—	a_4	a_3, a_5	a_0, a_1, a_3	a_0, a_5	Yes
C_1 down 10%	—	a_4, a_5	a_4, a_5	a_1, a_2, a_3	a_1, a_4	Yes
C_2 up 10%	—	a_2, a_3	a_1, a_2	a_2, a_3, a_4	a_0, a_4	Yes
C_3 down 15%	—	a_1, a_3	a_0, a_1, a_2	a_4, a_5	a_0, a_1	Yes
C_4 down 10%	—	a_0, a_1	a_1, a_2	a_2, a_3	a_2, a_5	Yes
C_5 up 5%	—	a_0, a_1	a_1, a_5	a_1, a_2	a_3, a_4	Yes
C_6 up 15%	—	a_3, a_4	a_1, a_2, a_4	a_3, a_4, a_5	a_1, a_2	Yes
C_7 up 15%	—	a_1, a_4	a_1, a_3, a_4	a_1, a_3, a_5	a_3, a_4	Yes

confidence level at each of these frequencies. The intersection of sets of fault sites at all the frequencies (and at DC) gives a fault site with much higher confidence level. That is, if the confidence of diagnosis of a fault site at one frequency is say P_i , then the resulting confidence level after diagnosis at all the frequencies is as follows [18]:

$$P = 1 - \prod_{i=1}^{i=N} (1 - P_i) \quad (24)$$

where N is the number of frequencies (including DC) at which the circuit is diagnosed.

Single parametric faults of the elliptic filter in Figure 5 were diagnosable with confidence levels up to 60% at each frequency. The resulting confidence level after fault deduction from the four frequencies at which it was diagnosed is about 98.9%. The diagnosis results are given in Table IV for several injected single parametric faults. Another observation worthy of mention here is that the cardinality of set of fault sites detected at frequencies close to cut-off frequency is greater than that at frequencies closer to DC. This can be attributed to higher sensitivity of coefficients to circuit parameters at these frequencies. As a result, fault coverage is better by observing coefficient drifts at frequencies close to f_c . However these frequencies tend to be unfavorable for diagnosis as more than one parameter is likely to have displaced the coefficients out of their respective hypercubes. We can overcome this by looking at the set of fault sites obtained at frequencies much lower than f_c (100Hz used here).

VII. PROBABILITY MOMENTS AS A CIRCUIT SIGNATURE

The function of a circuit under test (CUT) is represented as a transformation on the probability density function of its input excitation, which is a continuous random variable (RV) with Gaussian probability distribution in [24], [25]. Probability moments of the output, now a transformed RV, are used as metrics for testing catastrophic and parametric faults in circuit components. The proposed use of probability moments as test metrics with white noise excitation as input addresses three important problems of analog circuit test, namely, 1) it reduces complexity of input signal design, 2) increases resolution of fault detection, and 3) reduces production test cost as it has no area overhead and marginally reduces test time. We also propose diagnosis of catastrophic faults in the circuit elements based on the unique relationship between specific moments of the output and circuit elements. We present a theoretical analysis, test and diagnosis procedures and SPICE simulation results for the proposed scheme applied to a benchmark elliptic filter and a low noise amplifier. We are able to detect all catastrophic faults and single faults in components that deviate from their nominal value by just over 10%. We diagnose all catastrophic faults in the example circuits considered.

VIII. V-TRANSFORM AS A CIRCUIT SIGNATURE

Parametric fault testing of non-linear analog circuits based on a new mathematical transform called V-transform is introduced in [23], [32]. V-transform acts on the polynomial expansion of the circuit's input-output voltage transfer function. It primarily serves to: 1) make the polynomial coefficients monotonic, 2) reduce masking of parametric faults

TABLE IV
PARAMETRIC FAULT DIAGNOSIS WITH CONFIDENCE LEVELS $\approx 98.9\%$.

Injected fault	Diagnosed fault sites at					Deduced fault site
	DC	100Hz	900Hz	1000Hz	1100Hz	
R_1 down 15%	R_1, R_4	R_1	R_1, R_2	R_1, R_2, C_1	R_1, C_1	R_1
R_2 down 5%	R_2	R_2, C_1	R_2, R_3, C_1	R_2, R_3	R_2, C_1	R_2
R_3 up 10%	R_1, R_3	R_3, C_3	R_3, R_4, C_3	R_3	R_3, C_3	R_3
R_4 down 20%	R_1, R_4	R_1, R_4	R_2, R_4, C_1	R_1, R_2, R_4	R_1, R_2, R_4	R_4
R_5 up 15%	R_5	R_5, C_2	R_4, R_5	R_4, R_5, C_2	R_5, R_6, C_3	R_5
R_6 up 5%	—	R_6, C_2	R_6, R_7	R_6, C_2, C_4	R_6, C_2, C_3	R_6
R_7 down 10%	R_3, R_7	R_7, C_3	R_3, R_7	R_3, R_6, R_7	R_3, R_7, C_3	R_7
R_8 up 10%	—	R_6, R_8	R_8, R_9	R_6, R_8	R_8, R_9	R_8
R_9 down 5%	—	R_8, R_9	R_8, R_9	R_9, R_{10}	R_8, R_9	R_9
R_{10} up 15%	—	R_{10}	R_{10}, C_6	R_{10}	R_{10}, C_6	R_{10}
R_{11} down 10%	R_{11}, R_{12}	R_{11}	R_{11}, C_5	R_{11}, R_{12}	R_{11}, R_{12}, C_5	R_{11}
R_{12} down 15%	R_{11}, R_{12}	R_{11}, R_{12}	R_{12}, C_5	R_{12}, C_5	R_{12}, C_5, C_7	R_{12}
R_{13} up 5%	—	R_{13}, C_5	R_{13}, C_7	R_{13}, C_5, C_6	R_{13}, C_5	R_{13}
R_{14} up 20%	—	R_{14}	R_{14}, R_{15}	R_{14}, R_{15}	R_{14}, R_{15}	R_{14}
R_{15} up 5%	—	R_{13}, R_{15}	R_{14}, R_{15}	R_{14}, R_{15}, C_5	R_{14}, R_{15}	R_{15}
C_1 down 10%	—	R_2, C_1	R_2, C_1	R_2, C_1	R_2, C_1	C_1
C_2 up 10%	—	R_5, C_2	C_2, C_4	C_2	C_2	C_2
C_3 down 15%	—	C_3	R_3, C_3	C_3	C_3	C_3
C_4 down 10%	—	R_6, C_4	C_2, C_4	C_2, C_4	C_2, C_4	C_4
C_5 up 5%	—	C_5	R_{12}, C_5	C_5	C_5	C_5
C_6 up 15%	—	R_{10}, C_6	C_6, C_7	C_6, C_7	C_6, C_7	C_6
C_7 up 15%	—	C_6, C_7	C_7	C_6, C_7	C_6, C_7	C_7

due to process variation, and 3) increase the sensitivity of polynomial coefficients to the circuit parameter variation, thus enhancing diagnostic resolution. There in it is shown that the sensitivity of V-transform coefficients (VTC) with respect to circuit parameter variation is up to 3 to 5 times greater than the sensitivity of polynomial coefficients. Fault diagnosis of parametric faults under process variation using VTC is also presented. We also propose a scheme to distinguish between circuit specifications failures due to process variation versus manufacturing defects which manifest as parametric faults in [22]. A complete description of the V-transform and its application on example circuits such as elliptic filter and low noise amplifier is presented in [23], [27]. Our work in [26], [28] computes a bound on the achievable defect level and fault coverage in coefficient based parametric fault test schemes such as the above.

IX. ADAPTIVE TEST WITH SIGNATURES

Signatures proposed in this thesis can be used in a closed loop framework such that the correlation of signatures to circuit specifications is further boosted up. Authors in [36] propose an adaptive test methodology for analog circuits in the alternate/signature test framework. Our preliminary studies on this approach have shown the feasibility of this approach with in conjunction with the signatures such as polynomial coefficients and V-transform coefficients proposed in the previous chapters.

A. Overview

Block diagram in Figure 11 shows the high-level conceptual framework of the adaptive test methodology using circuit

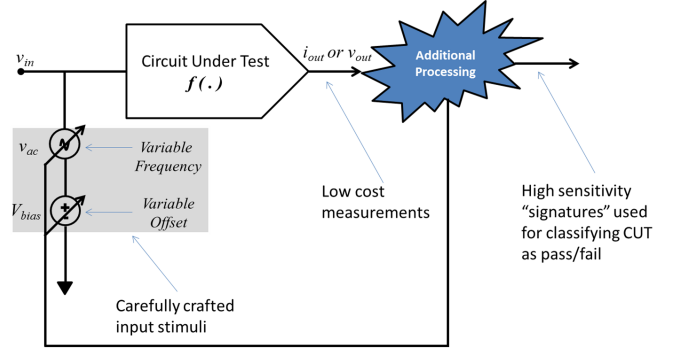


Fig. 11. Block diagram of the adaptive test system based on circuit signatures.

signatures. The circuit under test (CUT) is applied with a carefully crafted stimulus, whose output is then post-processed to generate the signatures such as polynomial coefficients or V-transform coefficients (proposed in previous chapters). The signatures are then used to compute correlation with the actual specification based on actual specification measurement of a small sampling of CUT at run-time. Based on the prevailing correlation, the input stimulus is tuned to achieve optimally sensitive signatures that has the highest degree of correlation to the circuit specification.

B. Preliminary Experiments

To our knowledge, a run-time, closed-loop tuning of the input stimulus to increase the correlation of the circuit signature to circuit specification for analog circuits has not been attempted before. Our initial experiments on a sample of 400 low noise amplifier [25], [27], [29] circuits show promising

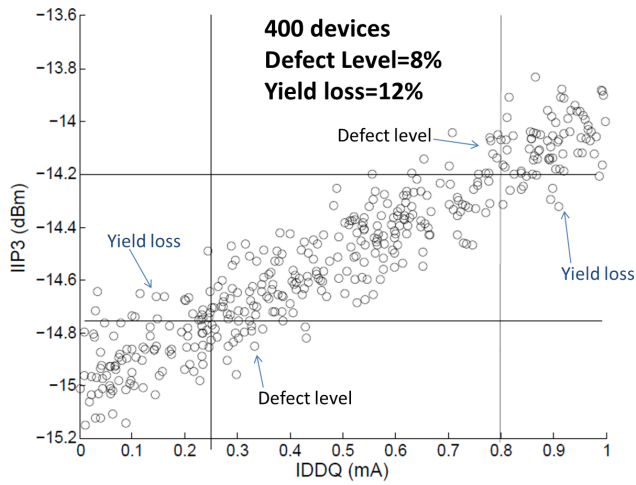


Fig. 12. Scatter plot of tested devices showing defect level and yield loss for the open loop signature test when the input stimulus is not tuned.

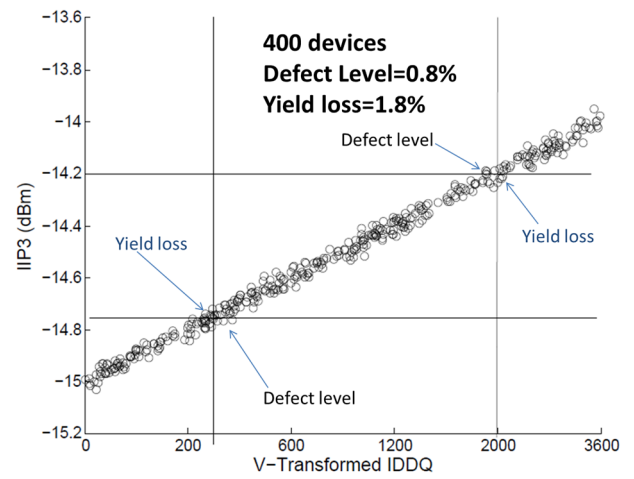


Fig. 13. Scatter plot of tested devices showing defect level and yield loss for the closed loop signature test when the input stimulus is adaptively tuned.

results on the possibility of using such closed-loop tuning on circuit stimulus to achieve high correlation with specification, which results in lower defect level and yield loss.

We compare Figures 12 and 13. Figure 13 shows the improved correlation between the signature, in this case, V-transform of supply current (I_{dd}), as opposed to just I_{dd} and the specification IIP3 as shown in Figure 12. The penalty paid in this process is the extra test-time required to process the signatures and compute the required adjustments to the input stimulus at run-time (for example at production). However, it turns out that even minor adjustments in the input stimulus parameters can give rich dividends in the amount of correlation achieved through such closed-loop tuning. Furthermore, the computation time required for computing the change in stimulus along with the time required to initiate the change in the input stimulus amounts to about 10% increase in the total test-time when compared to test-flows that do not use such closed form tuning. Table V shows a comparison of three techniques, namely: testing for the specification “as is,” using V-transform coefficients in open-loop, and using V-transform coefficients in closed-loop. Actual specification testing serves as the baseline case (or ideal scenario) for defect level (DL) and yield loss (YL). Notice that signatures taken in open-loop result in a DL and YL of 8% and 12% respectively. Having a closed-loop tuning of the stimulus improves DL and YL to 0.8% and 1.8% with a 5% time-penalty over the open-loop case. But both these techniques give close to a 100x improvement in test-time over the baseline case (of measuring actual specification). More experiments are needed to study how this procedure would scale when the number of CUT are large and any other inadequacies of this approach.

X. CONCLUSION

A new approach for testing non-linear circuits based on polynomial expansion of the circuit function has been pro-

TABLE V
COMPARISON OF DEFECT LEVEL, YIELD LOSS, AND TEST TIME FOR ACTUAL SPECIFICATION TEST, SIGNATURE TEST IN OPEN LOOP, AND SIGNATURE TEST IN CLOSED LOOP.

Test Method	Defect Level	Yield Loss	Test Time (per device)
Actual specification test	0%	0%	15s
Open loop signature test	8%	12%	100ms
Closed loop signature test	0.8%	1.8%	105ms

posed. Polynomial coefficients of the circuit function expanded at critical frequencies are capable of detecting and diagnosing circuit component faults as small as 5% for the example circuits considered. Circuit test signatures for increasing the component sensitivity to specification, namely V-transform; and simplifying input signal design effort, namely, probability moments are briefly discussed. Also, an adaptive framework for using these signatures and the consequent improvement in defect level and yield loss is demonstrated.

In proposing new signatures (polynomial coefficients and probability moments) and the sensitivity enhancement technique (V-transform) this research, on one hand, enhances the tool set of alternate test and, on the other hand, provides a bridge between the alternate [35]–[37] and model-based test [2] methods. In our future research, we plan to extend this bridge by combining specification-based tests [3], [14] and signatures together in the adaptive test framework proposed here for overall test cost minimization with given (acceptable) defect level and yield loss.

ACKNOWLEDGMENT

This research is supported in parts by the National Science Foundation Grants CCF-1116213 and IIP-0738088, and by the Wireless Engineering Research and Education Center at Auburn University.

REFERENCES

- [1] A. Abderrahman, E. Cerny, and B. Kaminska, "Optimization Based Multifrequency Test Generation for Analog Circuits," *Journal of Electronic Testing: Theory and Applications*, vol. 9, no. 1-2, pp. 59–73, Mar 1996.
- [2] N. Ben Hamida and B. Kaminska, "Multiple Fault Analog Circuit Testing by Sensitivity Analysis," *Journal of Electronic Testing: Theory and Applications*, vol. 4, no. 4, pp. 331–343, Nov. 1993.
- [3] M. L. Bushnell and V. D. Agrawal, *Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits*. Springer, 2000.
- [4] S. Chakravarty and P. J. Thadikaran, *Introduction to IDDQ Testing*. Springer, 1997.
- [5] S. Cherubal and A. Chatterjee, "Test Generation Based Diagnosis of Device Parameters for Analog Circuits," in *Proc. Design, Automation and Test in Europe Conf.*, 2001, pp. 596–602.
- [6] G. Devarayanadurg and M. Soma, "Analytical Fault Modeling and Static Test Generation for Analog ICs," in *Proc. International Conf. Computer-Aided Design*, Nov. 1994, pp. 44–47.
- [7] S. L. Farchy, E. D. Gadzheva, L. H. Raykovska, and T. G. Kouyoumdjiev, "Nullator-Norator Approach to Analogue Circuit Diagnosis Using General-Purpose Analysis Programmes," *International Journal of Circuit Theory and Applications*, vol. 23, no. 6, pp. 571–585, Dec. 1995.
- [8] R. K. Gulati and C. F. Hawkins, *IDDQ Testing of VLSI Circuits*. Springer, 1993.
- [9] Z. Guo and J. Savir, "Analog Circuit Test Using Transfer Function Coefficient Estimates," in *Proc. International Test Conf.*, Oct. 2003, pp. 1155–1163.
- [10] A. Halder, S. Bhattacharya, and A. Chatterjee, "Automatic Multitone Alternate Test Generation for RF Circuits Using Behavioral Models," in *Proc. International Test Conf.*, Nov. 2003, pp. 665–673.
- [11] R. Kondagunturi, E. Bradley, K. Maggard, and C. Stroud, "Benchmark Circuits for Analog and Mixed-Signal Testing," in *Proc. 20th International Conf. Microelectronics*, Mar. 1999, pp. 217–220.
- [12] E. Kreyzig, *Advanced Engineering Mathematics*. Wiley, 2005.
- [13] W. L. Lindermeir, H. E. Graeb, and K. J. Antreich, "Analog Testing by Characteristic Observation Inference," *IEEE Trans. Comp. Aided Design*, vol. 23, no. 6, pp. 1353–1368, June 1999.
- [14] M. Mahoney, *DSP Based Testing of Analog and Mixed-Signal Circuits*. IEEE Computer Society Press, 1987.
- [15] L. Milor and V. Visvanathan, "Detection of Catastrophic Faults in Analog Integrated Circuits," *IEEE Trans. Comp. Aided Design*, vol. 8, no. 6, pp. 114–130, June 1989.
- [16] N. Nagi, A. Chatterjee, A. Balivada, and J. A. Abraham, "Fault-Based Automatic Test Generator for Linear Analog Devices," in *Proc. International Conf. Computer Aided Design*, May 1993, pp. 88–91.
- [17] V. Panic, D. Milovanovic, P. Petkovic, and V. Litovski, "Fault Location in Passive Analog RC Circuits by Measuring Impulse Response," in *Proc. 20th International Conf. Microelectronics*, Sept. 1995, pp. 12–14.
- [18] A. Papoulis, *Probability, Random Variables, and Stochastic Processes*. McGraw-Hill, 1965.
- [19] T. L. Quarles, D. O. Pederson, A. R. Newton, A. L. Sangiovanni-Vincentelli, C. Wayne, and J. M. Rabaey, "The Spice Page," accessed June 23, 2013. <http://bwrcs.eecs.berkeley.edu/Courses/IcBook/SPICE/>.
- [20] R. Rajsuman, *IDDQ Testing for CMOS VLSI*. Artech House, 1995.
- [21] S. Sindia, *High Sensitivity Signatures for Test and Diagnosis of Analog, Mixed-Signal and Radio-Frequency Circuits*. PhD thesis, Auburn University, Alabama, USA, Aug. 2013.
- [22] S. Sindia, V. D. Agrawal, and V. Singh, "Distinguishing Process Variation Induced Faults from Manufacturing Defects in Analog Circuits using V-Transform Coefficients," in *Proc. 43rd IEEE Southeastern Symp. System Theory*, Mar. 2011, pp. 231–236.
- [23] S. Sindia, V. D. Agrawal, and V. Singh, "Non-Linear Analog Circuit Test and Diagnosis under Process Variation using V-Transform Coefficients," in *Proc. 29th IEEE VLSI Test Symp.*, May 2011, pp. 64–69.
- [24] S. Sindia, V. D. Agrawal, and V. Singh, "Test and Diagnosis of Analog Circuits Using Moment Generating Functions," in *20th IEEE Asian Test Symposium*, 2011, pp. 371–376.
- [25] S. Sindia, V. D. Agrawal, and V. Singh, "Testing Linear and Non-linear Analog Circuits using Moment Generating Functions," in *Proc. 12th IEEE Latin American Test Workshop*, Mar. 2011, pp. 1–6.
- [26] S. Sindia, V. D. Agrawal, and V. Singh, "Defect Level and Fault Coverage in Coefficient Based Analog Circuit Testing," *Journal of Electronic Testing: Theory and Applications*, vol. 28, no. 4, pp. 541–549, Aug. 2012.
- [27] S. Sindia, V. D. Agrawal, and V. Singh, "Parametric Fault Testing of Non-Linear Analog Circuits Based on Polynomial and V-Transform Coefficients," *Journal of Electronic Testing: Theory and Applications*, vol. 28, no. 5, pp. 757–771, Oct. 2012.
- [28] S. Sindia, V. Singh, and V. D. Agrawal, "Bounds on Defect Level and Fault Coverage in Linear Analog Circuit Testing," in *Proc. 13th VLSI Design and Test Symposium*, July 2009, pp. 410–421.
- [29] S. Sindia, V. Singh, and V. D. Agrawal, "Multi-Tone Testing of Linear and Nonlinear Analog Circuits Using Polynomial Coefficients," in *Proc. 18th IEEE Asian Test Symposium*, Nov. 2009, pp. 63–68.
- [30] S. Sindia, V. Singh, and V. D. Agrawal, "Polynomial Coefficient Based DC Testing of Non-Linear Analog Circuits," in *Proc. 19th ACM Great Lakes Symp. on VLSI*, May 2009, pp. 69–74.
- [31] S. Sindia, V. Singh, and V. D. Agrawal, "Polynomial Coefficient Based Multi-Tone Testing of Analog Circuits," in *Proc. North Atlantic Test Workshop*, May 2009, pp. 9–18.
- [32] S. Sindia, V. Singh, and V. D. Agrawal, "V-Transform: An Enhanced Polynomial Coefficient Based DC Test for Non-Linear Analog Circuits," in *Proc. of 8th IEEE East West Design-Test Symp.*, Sept. 2009, pp. 283–286.
- [33] S. Sindia, V. Singh, and V. D. Agrawal, "Parametric Fault Diagnosis of Nonlinear Analog Circuits Using Polynomial Coefficients," in *Proc. 23rd International Conf. VLSI Design*, Jan. 2010, pp. 288–293.
- [34] M. Slamani and B. Kaminska, "Analog Circuit Fault Diagnosis Based on Sensitivity Computation and Functional Testing," *IEEE Design & Test of Computers*, vol. 19, no. 1, pp. 30–39, 1992.
- [35] H.-G. Stratigopoulos and Y. Makris, "Error Moderation in Low-Cost Machine-Learning-Based Analog/RF Testing," *IEEE Transactions on Computer-Aided Design*, vol. 27, no. 2, pp. 339–351, Feb. 2008.
- [36] H.-G. Stratigopoulos and S. Mir, "Adaptive Alternate Analog Test," *IEEE Design & Test of Computers*, vol. 29, no. 4, pp. 71–79, 2012.
- [37] P. N. Variyam, S. Cherubal, and A. Chatterjee, "Prediction of Analog Performance Parameters Using Fast Transient Testing," *IEEE Transactions on Computer-Aided Design*, vol. 21, no. 3, pp. 349–361, Mar. 2002.