

# A Tutorial on Test Power

Vishwani D. Agrawal  
Auburn University  
Auburn, AL 36849, USA  
+1 334-844-1853

vagrawal@eng.auburn.edu

## ABSTRACT

Both average power and peak power specifications of a circuit pose serious problems for the prevalent test methods like scan and built-in self-test. This tutorial discusses the problems and solutions for minimizing power dissipation in these test procedures. Hardware approaches and test vector optimization methods are outlined. Power-constrained testing of core-based systems is discussed. Finally, an open problem of finding an efficient test for verifying the power specification of a system is formulated.

Today's electronic systems are complex, fast, and energy efficient. Power is a circuit design criteria, added to the previous list of area, delay and testability. Controlling test power and minimizing test time requires tradeoffs. Design for testability methods like scan and random-pattern self-test use non-functional test inputs that must conform to circuit specifications on average power (energy consumption) and peak power. Test power has thus become an active area of research, innovation and practice.

Electronic circuits should dissipate no more power or energy than they are designed for. In testing of circuits cost and quality are the requirements and high fault coverage can lead to long, often non-functional, test sequences. Such tests generate substantially higher signal activity and can potentially cause an otherwise good circuit to fail due to excessive power dissipation. Tests are, therefore, run at a slower speed, incurring longer test time and higher test cost. This extra cost of testing does not completely solve the test power problem. The slow speed test can contain high activity vectors that would cause excessive supply current surges. Once again a perfectly good circuit can potentially fail during test due to conditions such as power droop, ground bounce and hot spots.

## Categories & Subject Descriptors

B.7.1 [Hardware]: Integrated Circuits – *VLSI (very large scale integration)*, B.8.1 [Hardware]: Performance and Reliability – Reliability, Testing and Fault-Tolerance

## General Terms

Design, Measurement, Reliability, Verification

## Keywords

Low-power design, Testing

**Vishwani D. Agrawal** is James J. Danaher Professor of Electrical and Computer Engineering at Auburn University, Alabama. He has over thirty years of industry and university experience at Bell Labs, Murray Hill, NJ; Rutgers University, New Brunswick, NJ; TRW, Redondo Beach, CA; IIT, Delhi, India; EG&G, Albuquerque, NM; and ATI, Champaign, IL. His research areas are VLSI testing and low-power design. He obtained a BE from Indian Institute of Technology, Roorkee, India, in 1964; ME from Indian Institute of Science, Bangalore, India, in 1966; and PhD in from University of Illinois, Urbana-Champaign, in 1971. He has published over 300 papers, has coauthored five books and holds thirteen United States patents. His textbook, *Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits*, co-authored with M. L. Bushnell, was published in 2000. He is the founder and Editor-in-Chief (1990- ) of the *Journal of Electronic Testing: Theory and Applications*, and a past Editor-in-Chief (1985-87) of the *IEEE Design & Test of Computers* magazine. Since 2003, he has served on the Editorial Board of the *IEEE Transactions on VLSI Systems*. He is the Founder and Consulting Editor of the *Frontiers in Electronic Testing* Book Series of Springer. He is a co-founder of the *International Conference on VLSI Design*, and the *International Workshops on VLSI Design and Test*, held annually in India. He was the invited Plenary Speaker at the *1998 International Test Conference*, Washington D.C., and the Keynote Speaker at the *Ninth Asian Test Symposium*, held in Taiwan in December 2000. During 1989 and 1990, he served on the Board of Governors of the IEEE Computer Society. He has received *eight* Best Paper Awards and *two* Honorable Mention Paper Awards. He received the Life-Time Achievement Award (2006) of the VLSI Society of India, the Harry H. Goode Memorial Award (1998) of the IEEE Computer Society, and the Distinguished Alumnus Award (1993) of the University of Illinois at Urbana-Champaign. Dr. Agrawal is a Fellow of the IETE-India (elected in 1983), a Fellow of the IEEE (elected in 1986) and a Fellow of the ACM (elected in 2003). He served on advisory boards of ECE Departments at University of Illinois, New Jersey Institute of Technology, and the City College of the City University of New York. See his website <http://www.eng.auburn.edu/~vagrawal>