A Tutorial on Test Power

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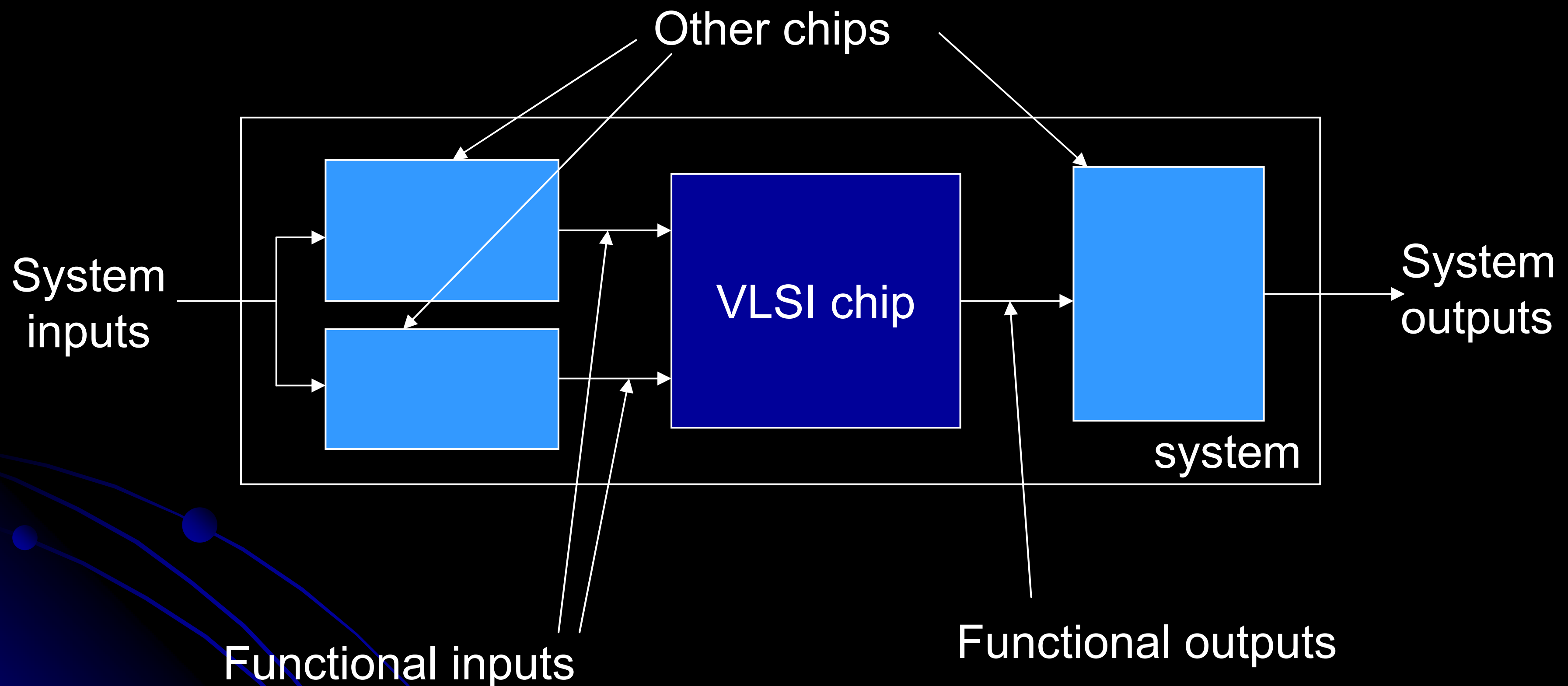
Power Considerations in Design

- A circuit is designed for certain function. Its design must allow the power consumption necessary to execute that function.
- Power buses are laid out to carry the maximum current necessary for the function.
- Heat dissipation of package conforms to the average power consumption during the intended function.
- Layout design and verification must account for "hot spots" and "voltage droop" – delay, coupling noise, weak signals.

Testing Differs from Functional Operation

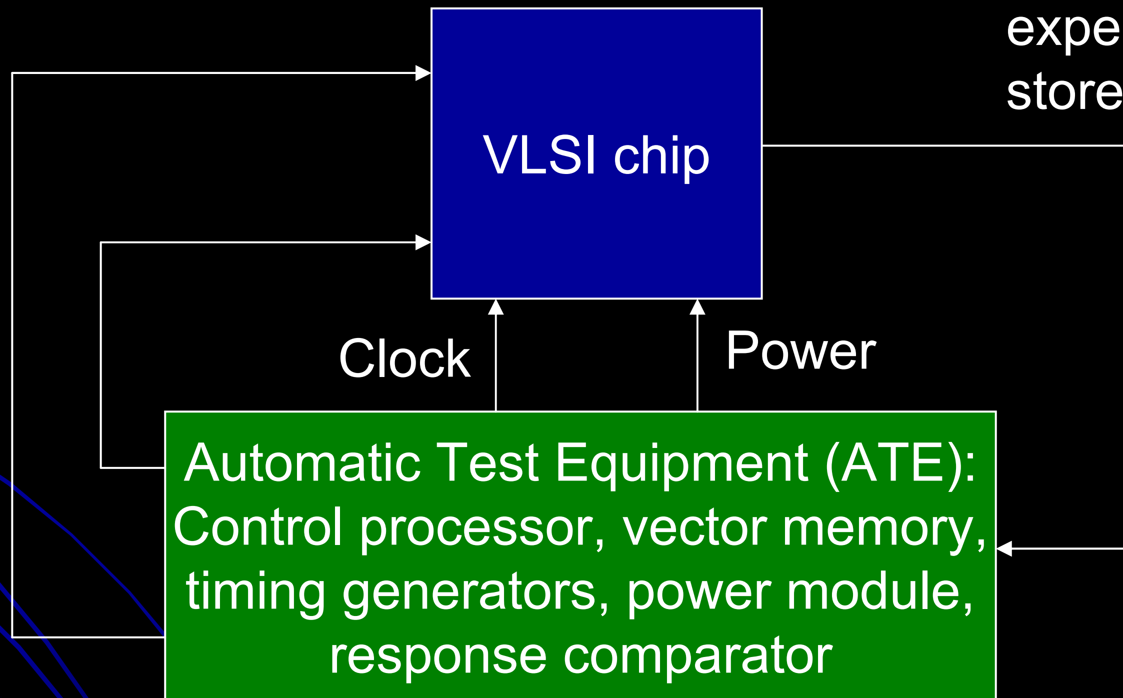


Basic Mode of Testing

Packaged or unpackaged device under test (DUT)

DUT output for comparison with expected response stored in ATE

Test vectors: Pre-generated and stored in ATE

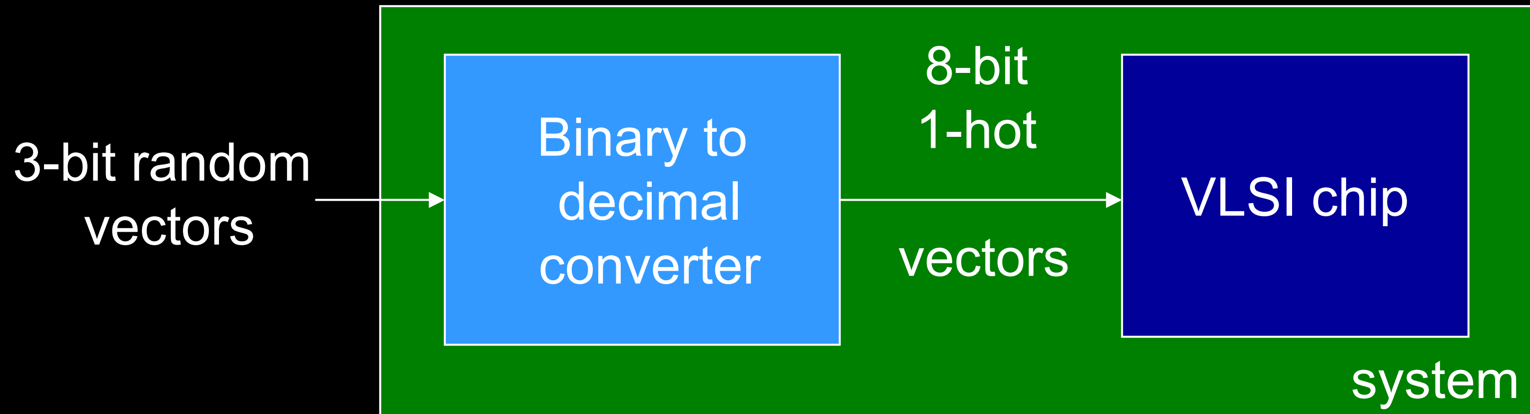


Functional Inputs vs. Test Vectors

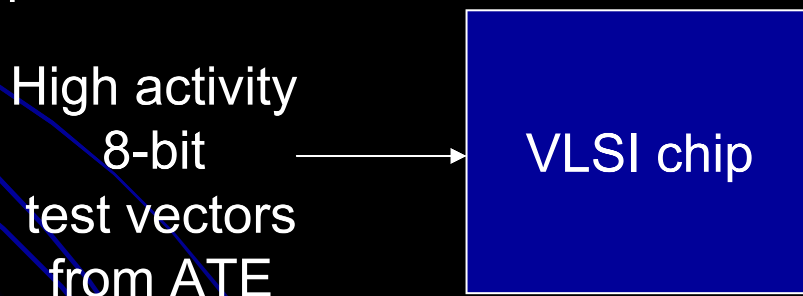
- **Functional inputs:**
  - Functionally meaningful signals
  - Generated by circuitry
  - Restricted set of inputs
  - May have been optimized to reduce logic activity and power
- **Test vectors:**
  - Functionally irrelevant signals
  - Generated by software to test modeled faults
  - Can be random or pseudorandom
  - May be optimized to reduce test time; can have high logic activity
  - May use testability logic for test application

An Example

VLSI chip in system operation



VLSI chip under test



Comb. Circuit Power Optimization

- Given a set of test vectors
- Reorder vectors to minimize the number of transitions at primary inputs

01010101
00110011
00001111
11 transitions

Combinational circuit (tested by exhaustive vectors)

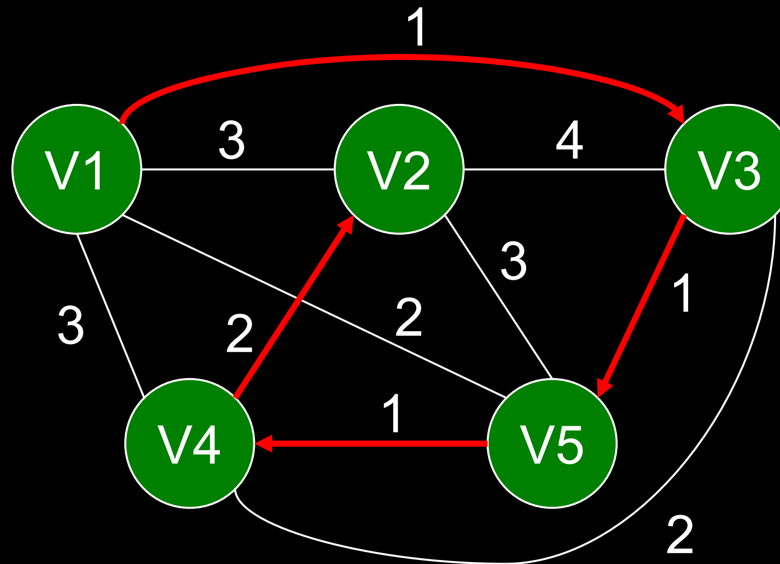
Rearranged vector set
01111000
00110011
00011110
produces 7 transitions

Reducing Comb. Test Power

Original tests:

V1	V2	V3	V4	V5
1	1	0	0	0
1	0	1	0	0
1	0	1	0	1
1	0	1	1	1

10 input transitions



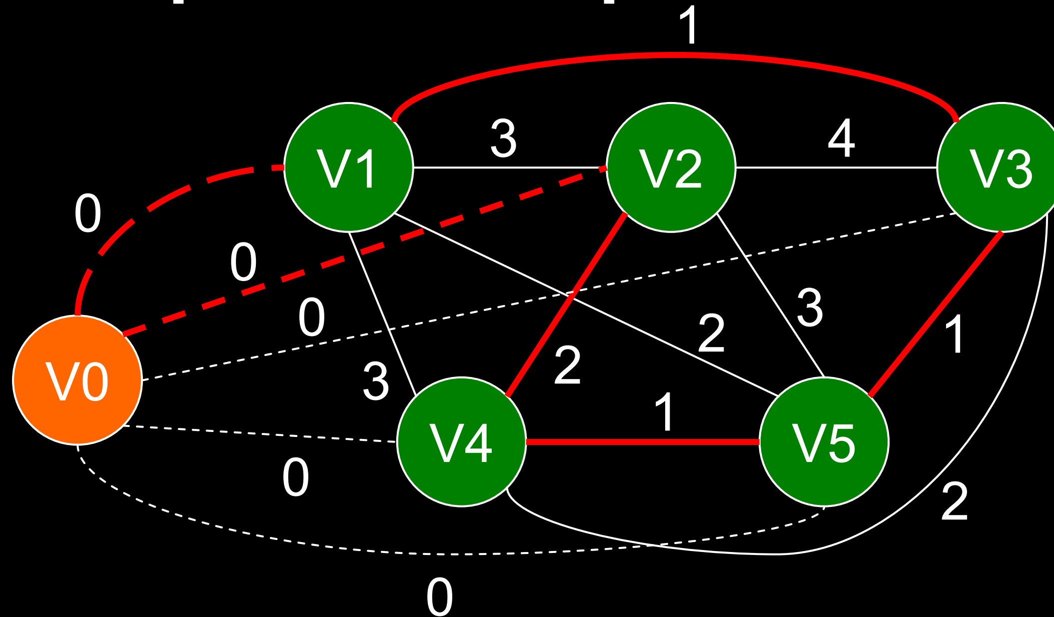
Reordered tests:

V1	V3	V5	V4	V2
1	0	0	0	1
1	1	0	0	0
1	1	1	0	0
1	1	1	1	0

5 input transitions

Traveling salesperson problem (TSP) finds the shortest distance closed path (or cycle) to visit all nodes exactly once. *But, we need an open loop solution.*

Open-Loop TSP



- Add a node V0 at distance 0 from all other nodes.
- Solve TSP for the new graph.
- Delete V0 from the solution.

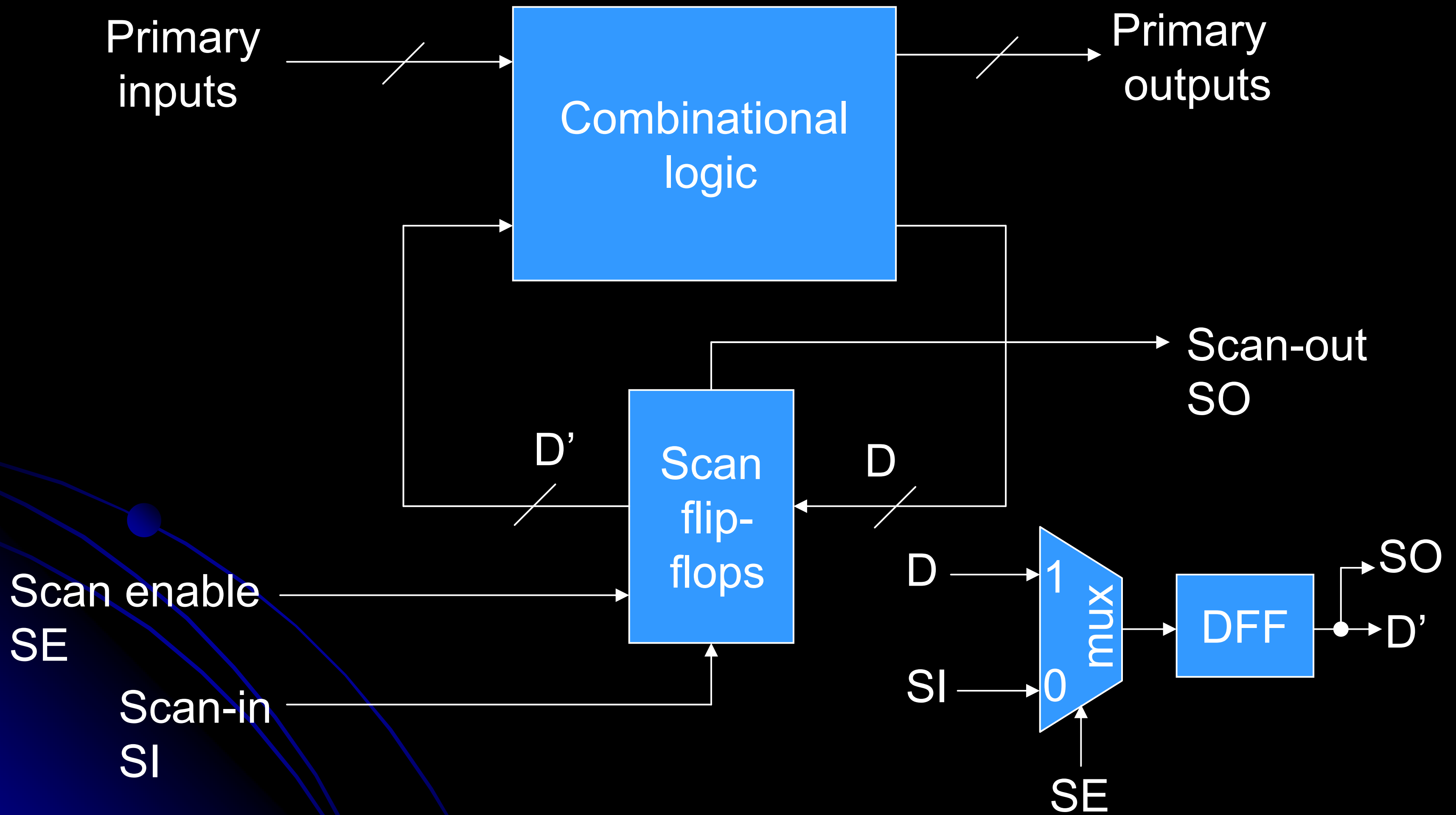
Combinational Vector Ordering

- TSP has exponential complexity; good heuristics are available.
- For other extensions:
  - V. Dabholkar, S. Chakravarty, I Pomeranz and S. Reddy, "Techniques for Minimizing Power Dissipation in Scan and Combinational Circuits During Test Application," *IEEE Trans. CAD*, vol. 17, no. 12, pp. 1325-1333, Dec. 1998.
- Typical average power saving:
  - 30-50%
  - 50-60% with vector repetition (to satisfy peak power)
  - ? ? ? With inserted vectors (to satisfy peak power)

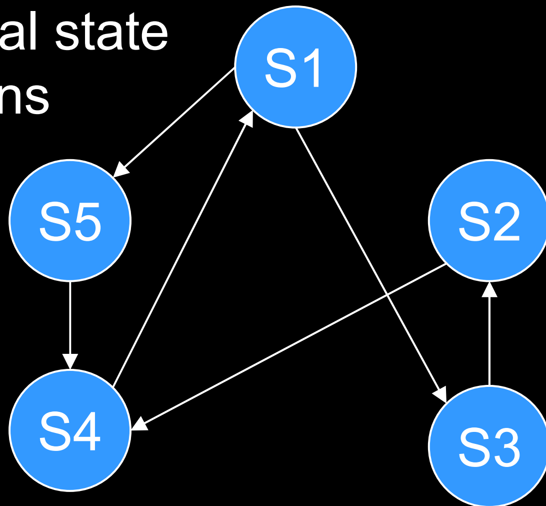
Traveling Salesperson Problem

- A. V. Aho, J. E. Hopcroft anf J. D. Ullman, *Data Structures and Algorithms*, Reading, Massachusetts: Addison-Wesley, 1983.
- E. Horowitz and S. Sahni, *Fundamentals of Computer Algorithms*, Computer Science Press, 1984.
- B. R. Hunt, R. L. Lipsman, J. M. Rosenberg, K. R. Coombes, J. E. Osborn and G. J. Stuck, *A Guide to MATLAB for Beginners and Experienced Users*, Cambridge University Press, 2006.

Scan Testing



Example: State Machine



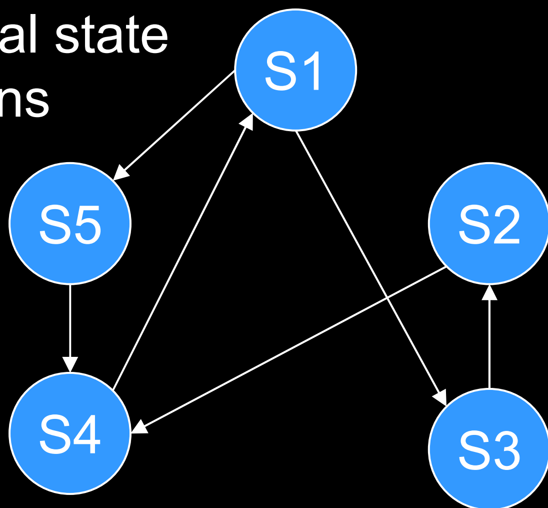
State encoding
S1 = 000
S2 = 001
S3 = 010
S4 = 011
S5 = 100

Functional transitions

State transition	Comb. State input changes/clock
000 → 010	1
000 → 100	1
001 → 011	1
010 → 001	2
011 → 000	2
100 → 011	3 (Peak)
Av. transitions	1.667

Reduced Power Design

Functional state transitions

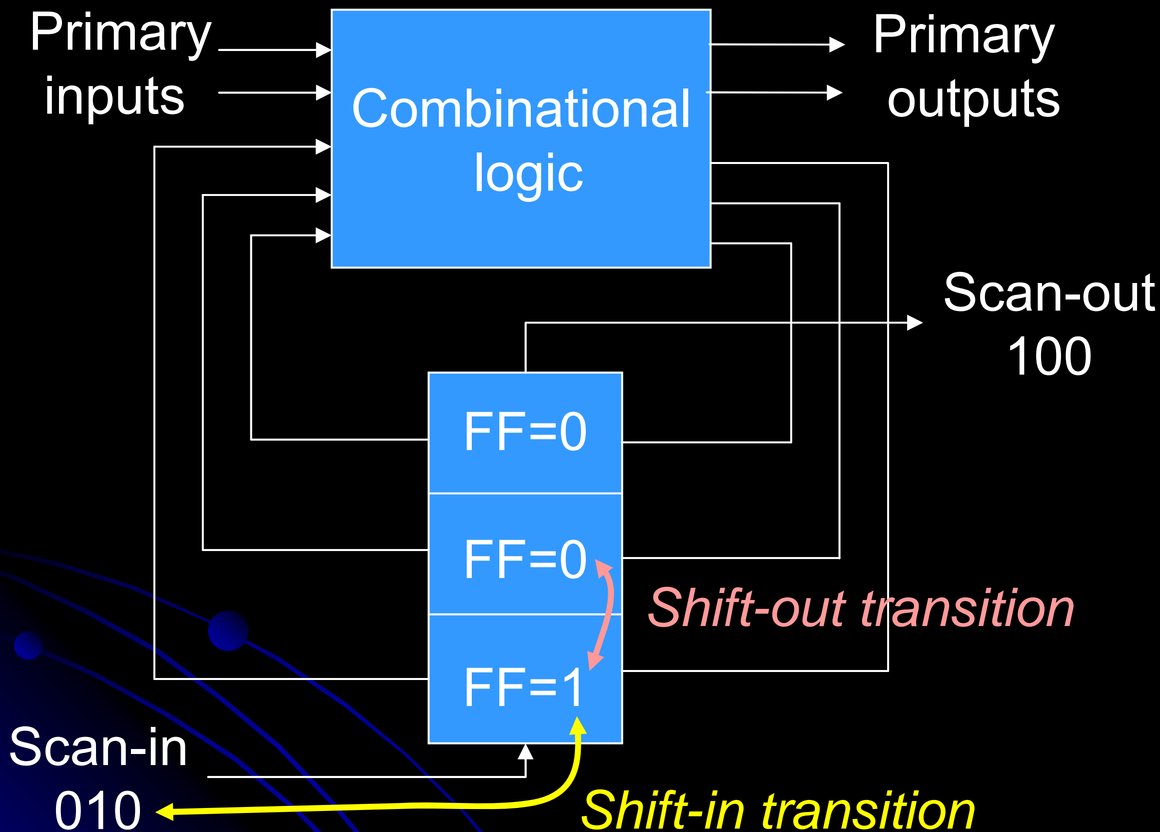


Reduced power state encoding
S1 = 000
S2 = 011
S3 = 001
S4 = 010
S5 = 100

Functional transitions

State transition	Comb. State input changes/clock
000 → 001	1
000 → 100	1
011 → 010	1
001 → 011	1
010 → 000	1
100 → 010	2 (Peak)
Av. transitions	1.167 (– 30%)

Scan Testing: Shift-in, Shift-out

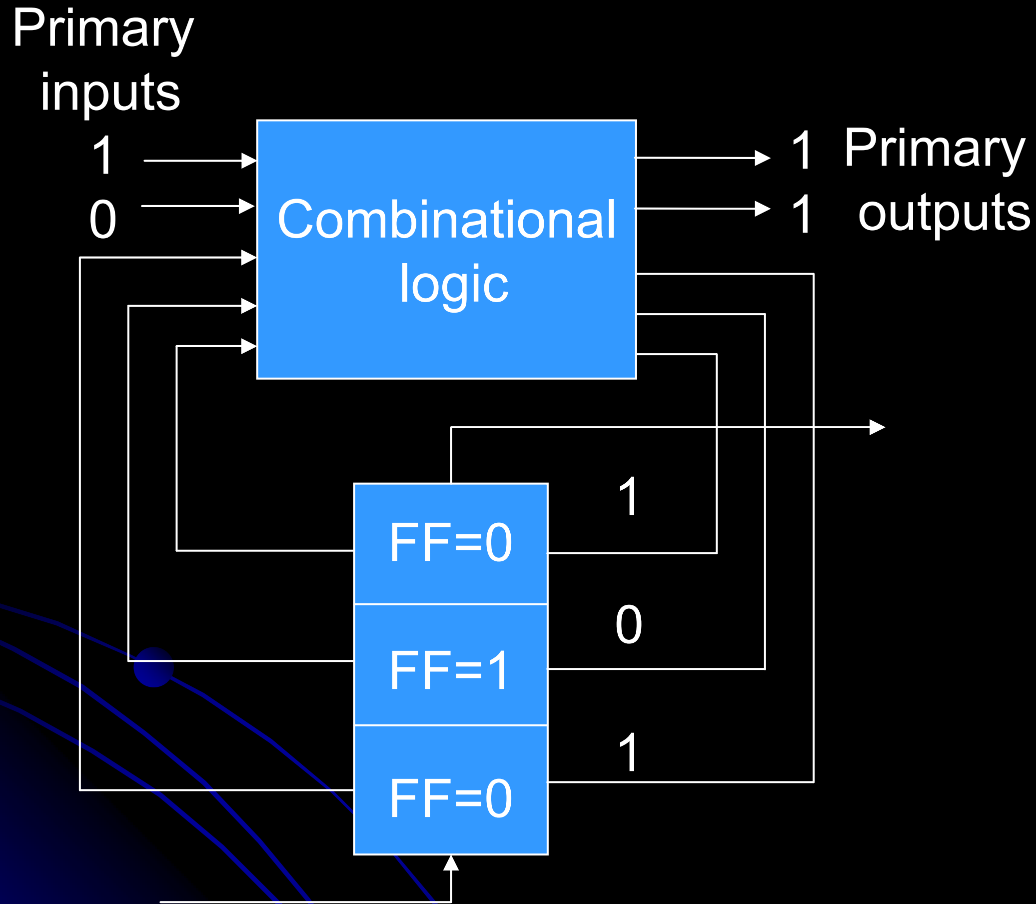


Scan transitions

State transition	Per clock state changes
100 → 010	2
010 → 101	3
101 → 010	3
All transitions	8

Shift-in transitions = Σ (scan chain length – position of transition)
Shift-out transitions = Σ (position of transition)

Scan Testing: Capture



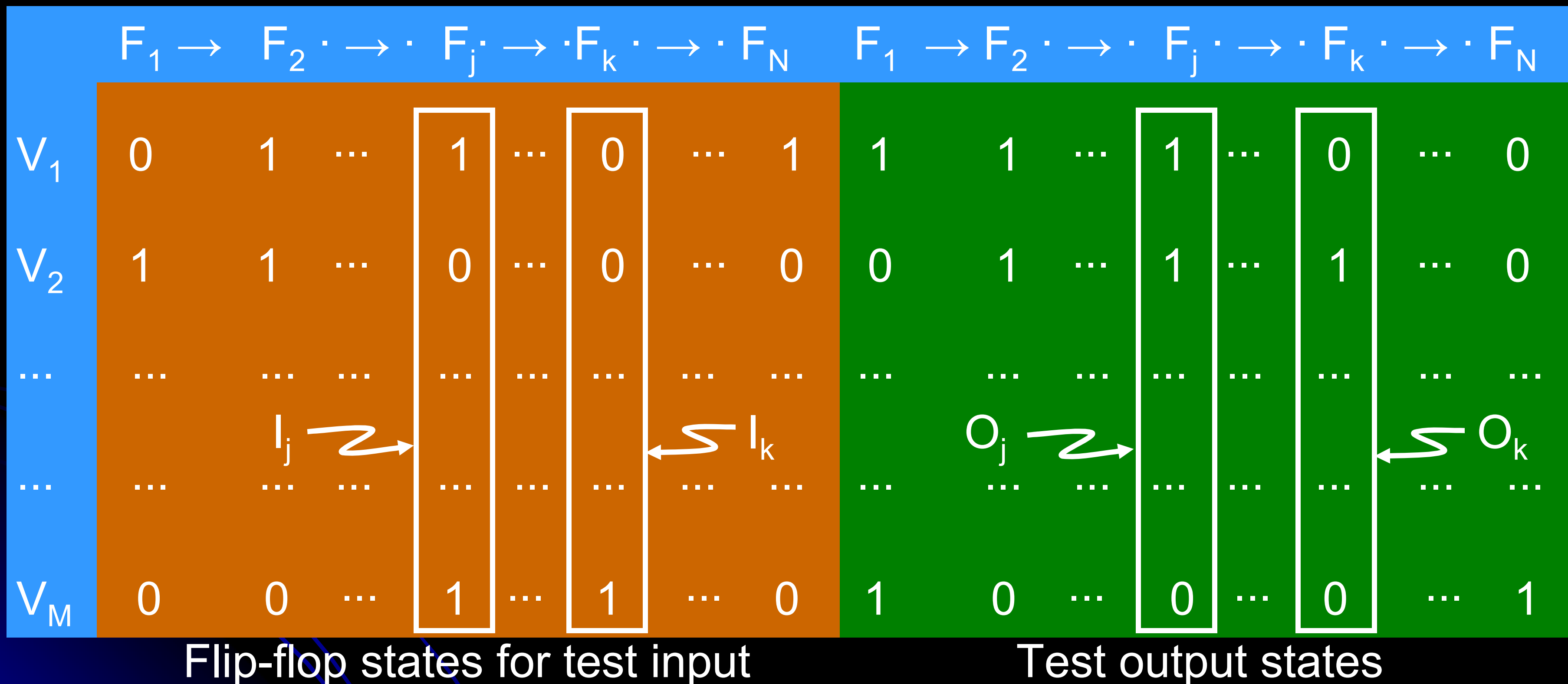
Capture transitions: 3
Note that 101 *is not a functional state in the reduced power state encoding.*

Dynamic Power of Scan Test

- Capture power can be reduced:
  - A vector generation problem
  - A vector ordering problem
- Shift-in and shift-out power is reduced by *vector ordering* and *scan chain ordering*
  - Construct a flip-flop node graph; edges weighted with shift in/out activity
  - Find shortest distance Hamiltonian paths between all node pairs
  - Select the path that minimizes shift power

Shift-in and Shift-out Matrices

N Scan flip-flops: F_1 through F_N; M vectors: V_1 through V_M

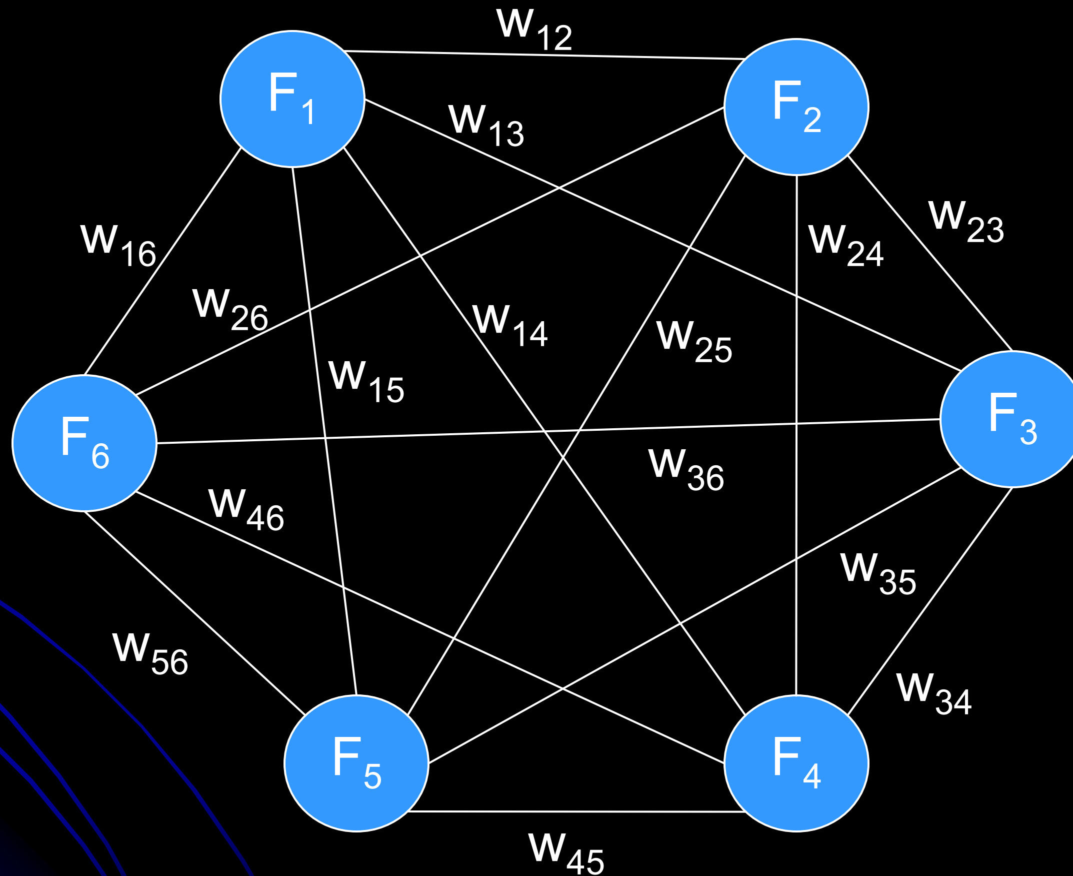


Flip-flop states for test input

Test output states

A Complete Graph

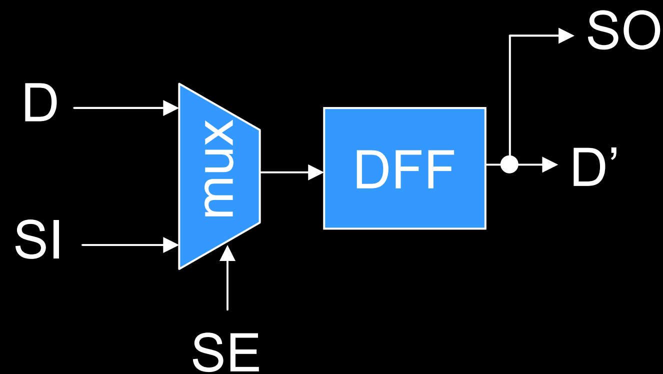
w_{jk} = Hamming(I_j, I_k) + Hamming(O_j, O_k)



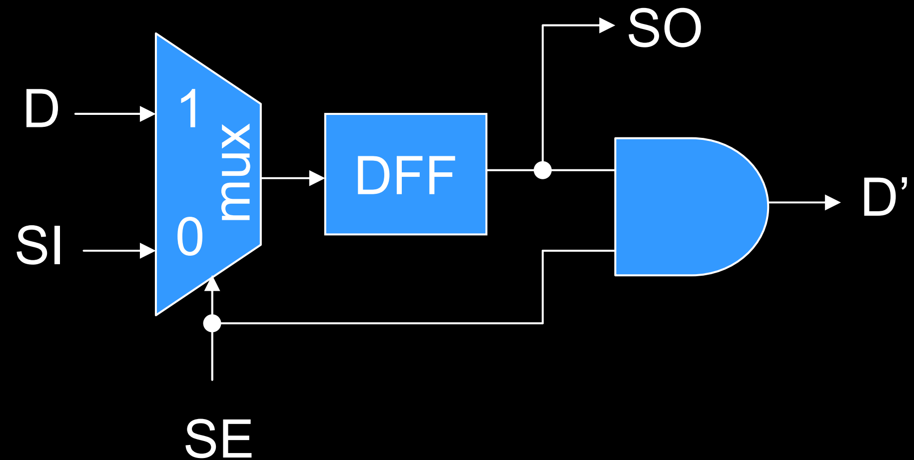
Graph Solutions for Scan Power

- High complexity of Hamiltonian path finding requires use of heuristics.
- Typical power saving: 10-20%
- Y. Bonhomne, P. Girard, Landrault, and S. C. Pravossoudovtich, “Power Driven Chaining of Flip Flops in Scan Architectures,” *Proc. International Test Conf.*, 2002, pp. 796–803.
- Y. Bonhomne, P. Girard, L. Guiller, Landrault, and S. C. Pravossoudovtich, “Power-Driven Routing-Constrained Scan Chain Design,” *J. Electronic Testing: Theory and Applications,* vol. 20, no. 6, pp. 647–660, Dec. 2004.

Low Power Scan Flip-Flop

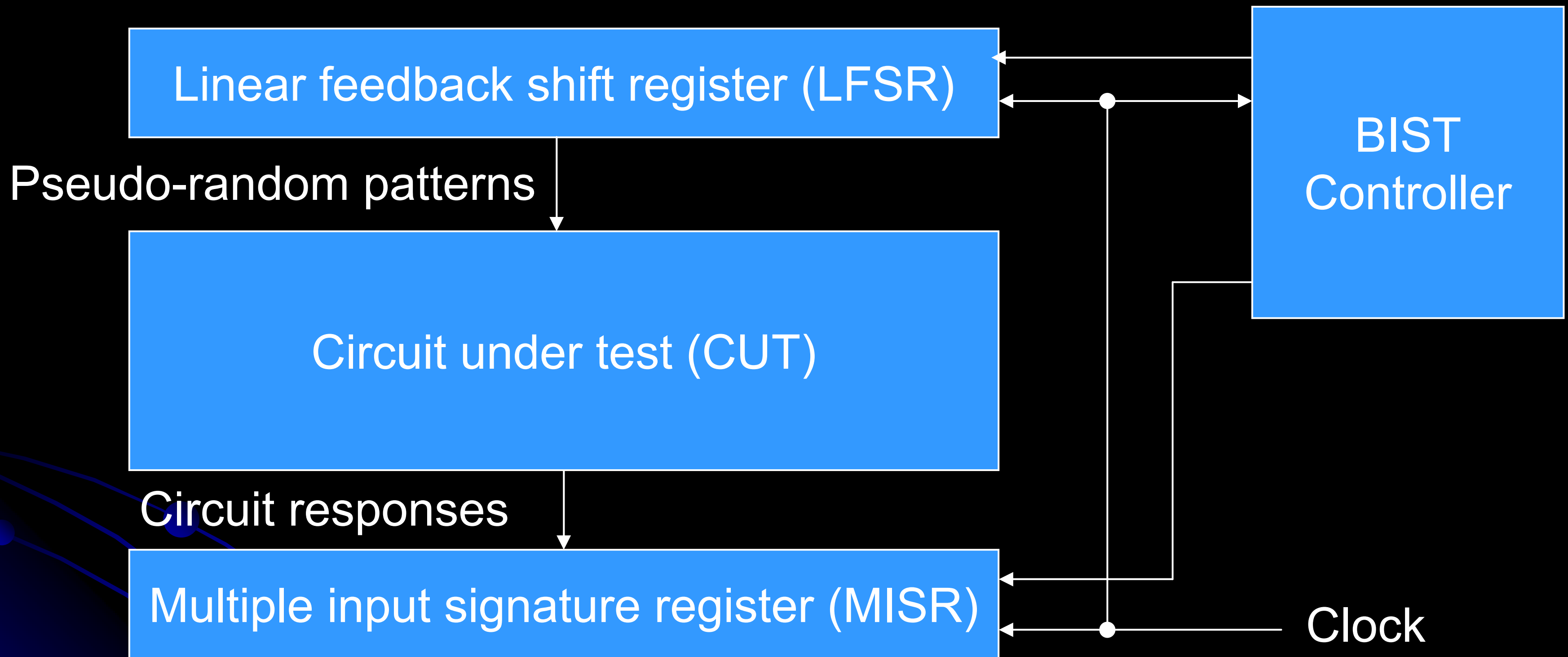


Scan FF cell



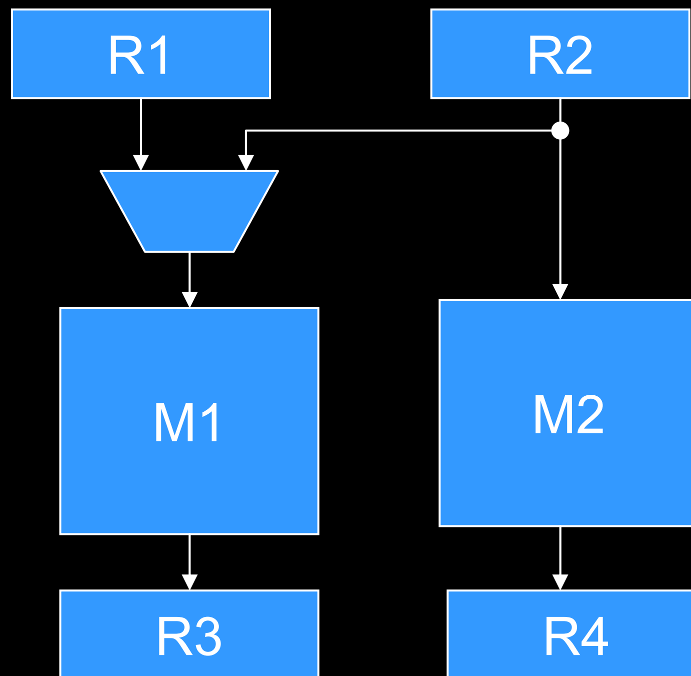
Low power scan FF cell

Built-In Self-Test (BIST)



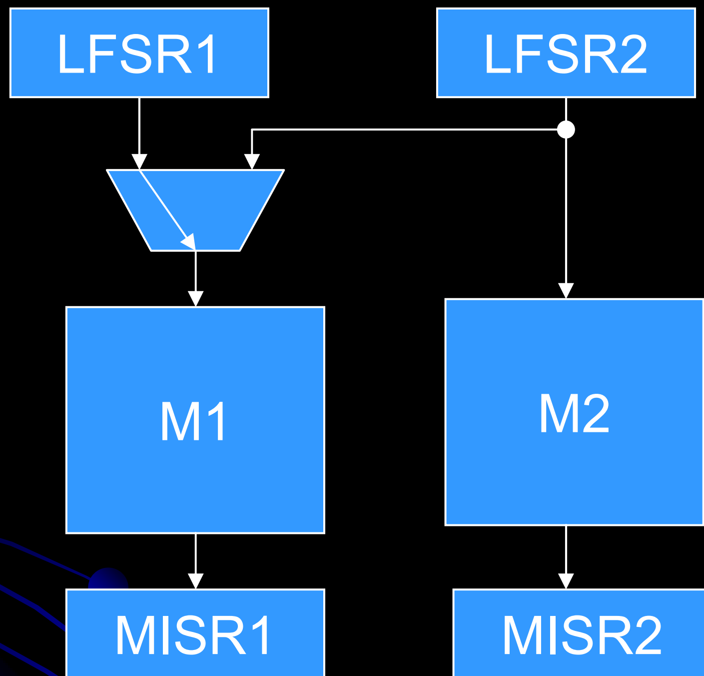
C. E. Stroud, *A Designer's Guide to Built-In Self-Test*, Boston: Springer, 2002.

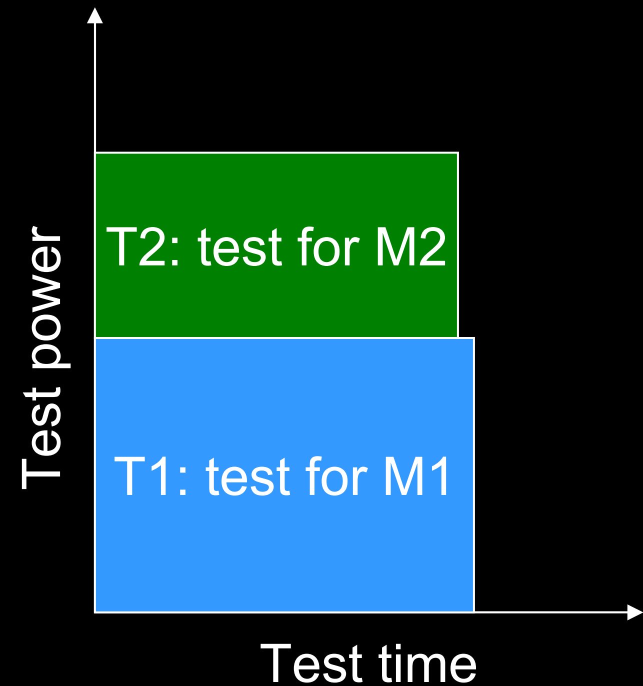
Test Scheduling Example



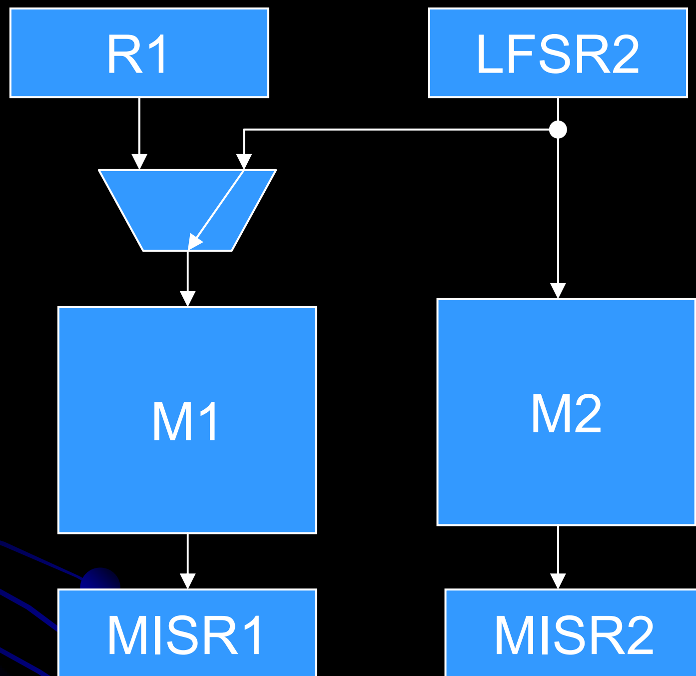
A datapath

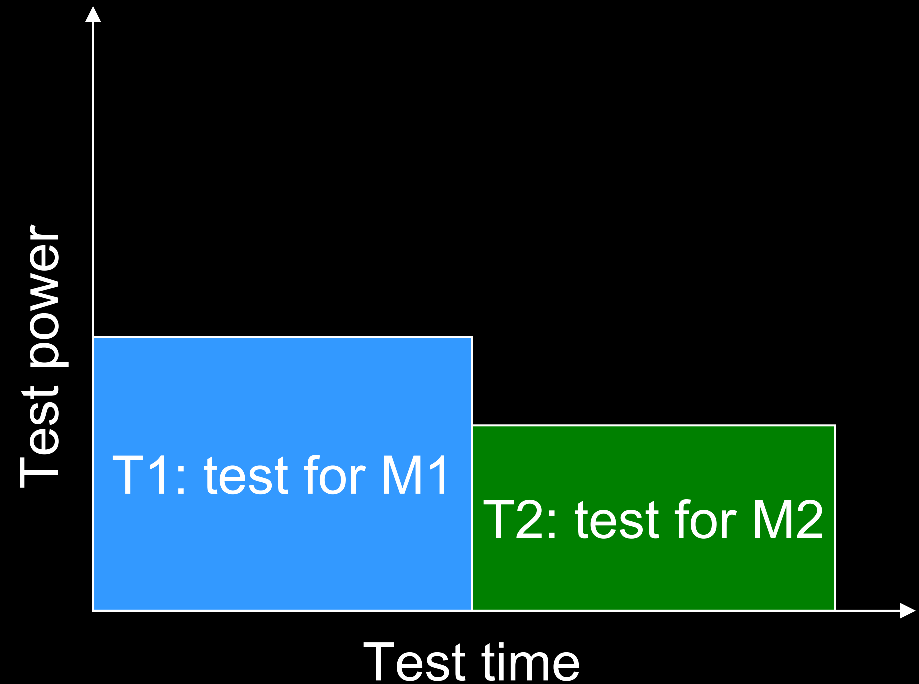
BIST Configuration 1: Test Time





BIST Configuration 2: Test Power

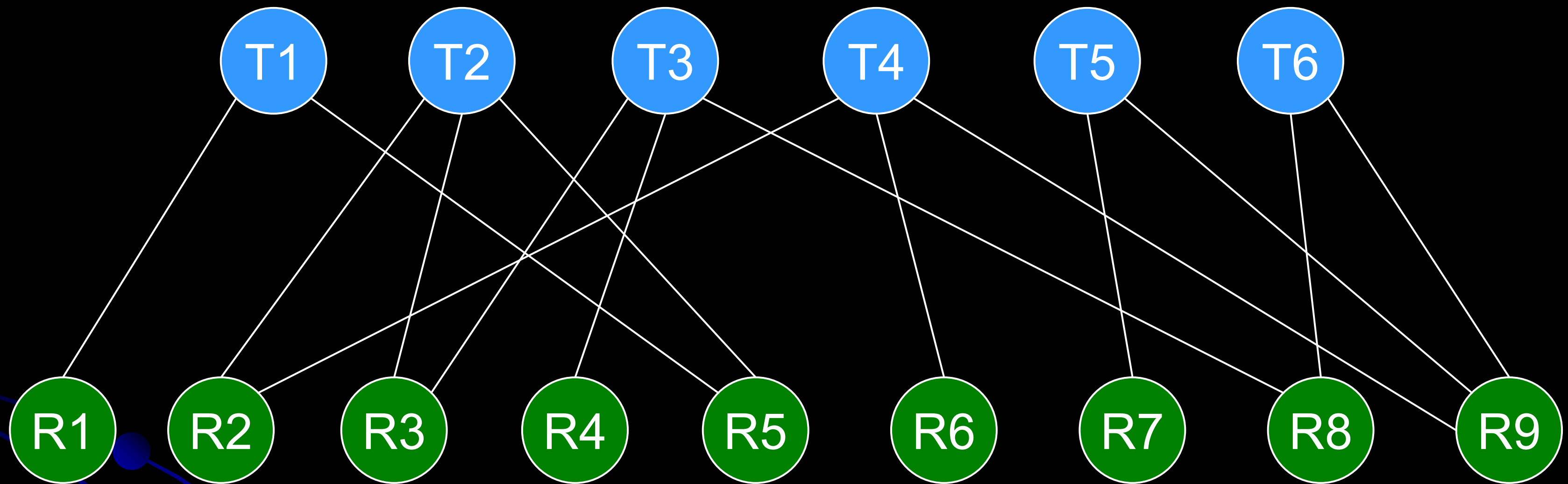




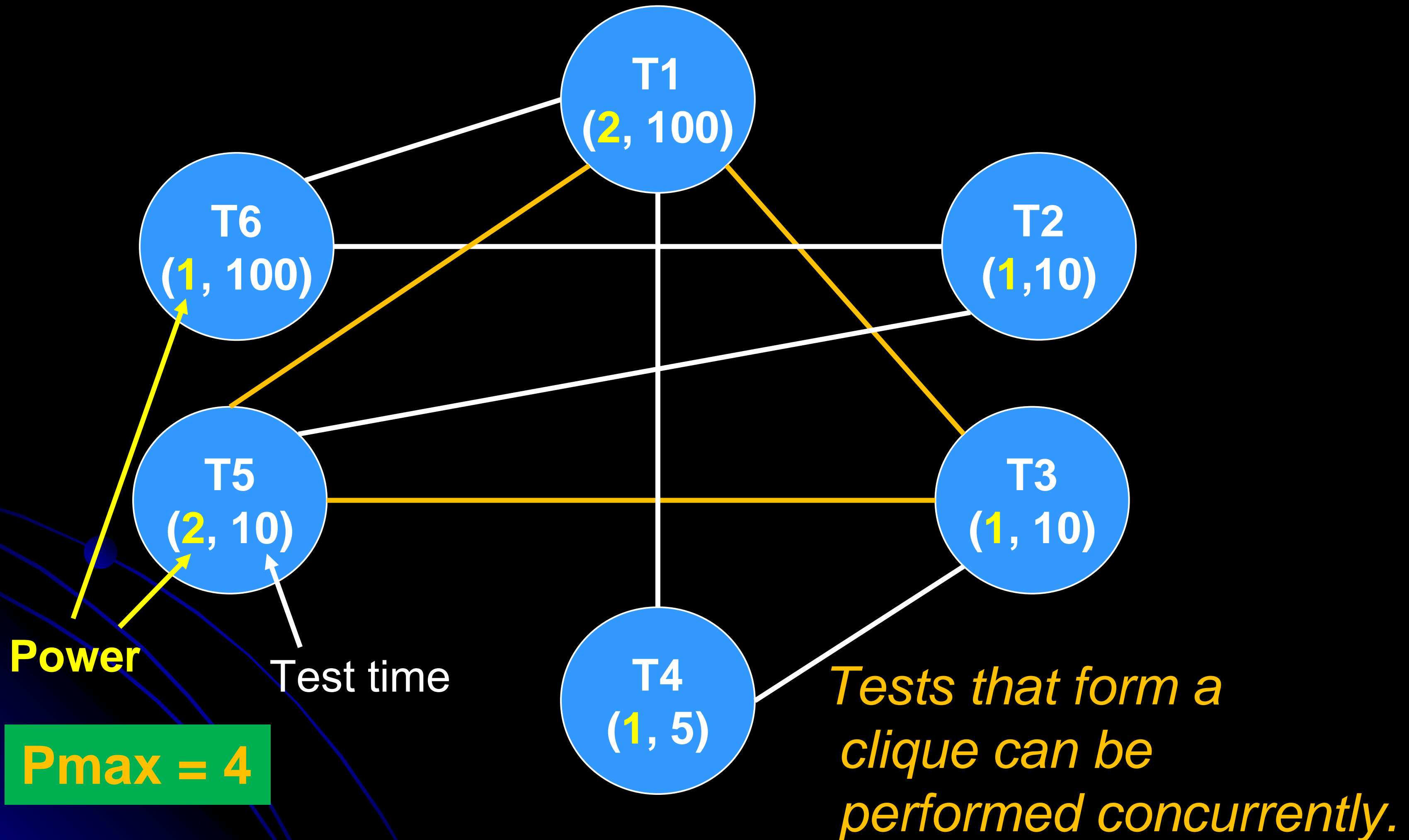
Testing of MCM and SOC

- Test resources: Typically registers and multiplexers that can be reconfigured as test pattern generators (e.g., LFSR) or as output response analyzers (e.g., MISR).
- Test resources (R1, . . .) and tests (T1, . . .) are identified for the system to be tested.
- Each test is characterized for test time, power dissipation and resources it requires.

Resource Allocation Graph



Test Compatibility Graph (TCG)



Find All Cliques in TCG

CLIQUE NO. i	TEST NODES	TEST LENGTH, Li	POWER, Pi
1	T1, T3, T5	100	5
2	T1, T3, T4	100	4
3	T1, T6	100	3
4	T1, T5	100	4
5	T1, T4	100	3
6	T1. T3	100	3
7	T2, T6	100	2
8	T2, T5	10	3
9	T3, T5	10	3
10	T3, T4	10	2
11	T1	100	2
12	T2	10	1
13	T3	10	1
14	T4	5	1
15	T5	10	2
16	T6	100	1

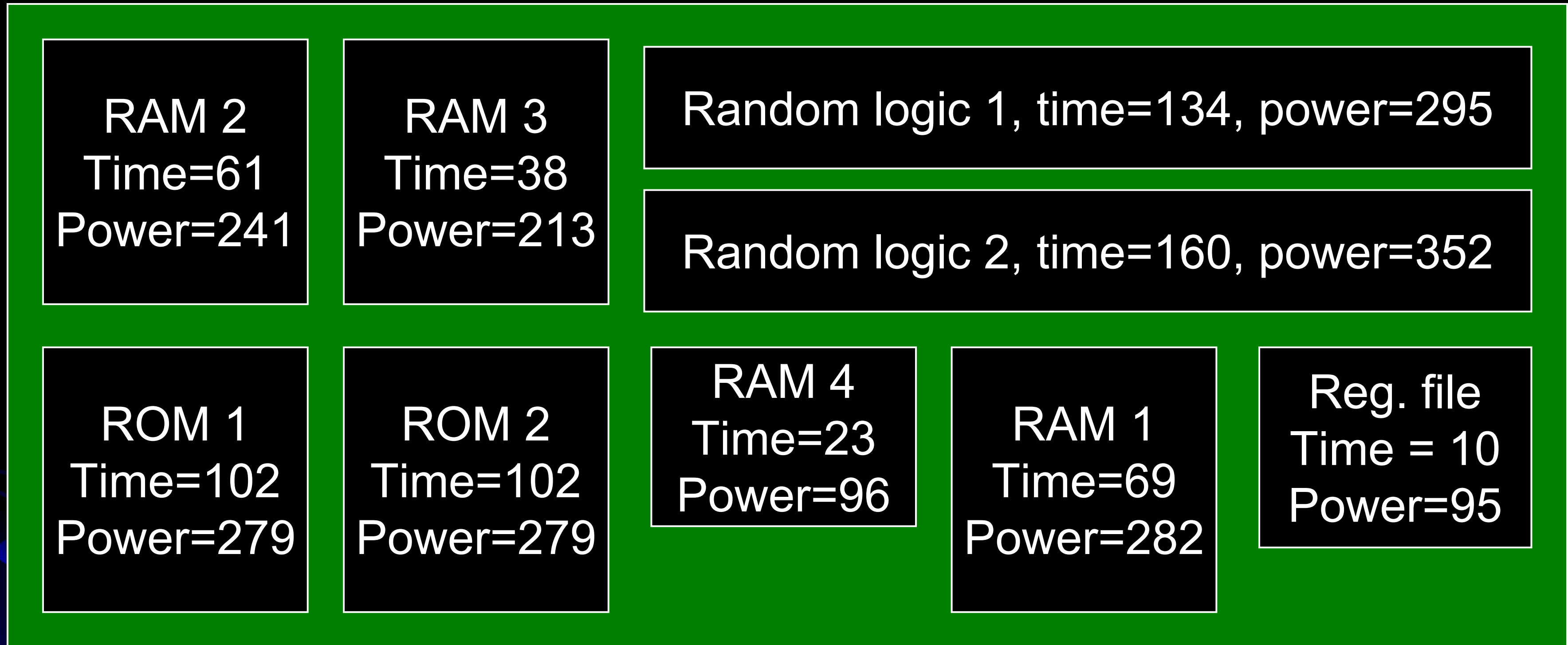
Integer Linear Program (ILP)

- For each clique (test session) i, define:
  - Integer variable, xi = 1, test session selected, or xi = 0, test session not selected.
  - Constants, Li = test length, Pi = power.
- Constraints to cover all tests:
  - T1 is covered if $x1+x2+x3+x4+x5+x6+x11 \geq 1$
  - Similar constraint for each test, Tk
- Constraints for power: $Pi \times xi \leq Pmax$

ILP Objective and Solution

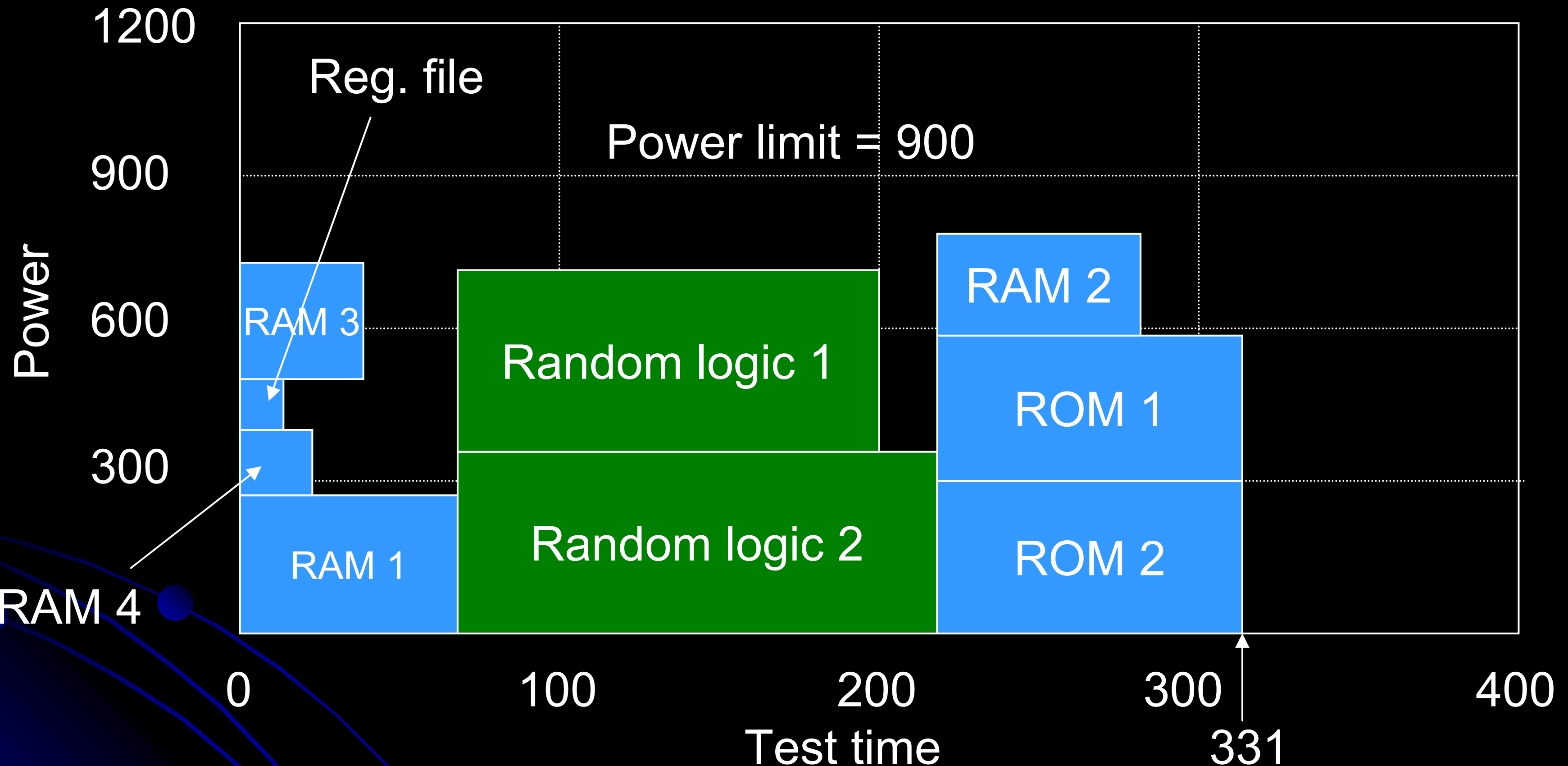
- Objective function:
  - Minimize $\sum_{\text{all cliques}} Li \times xi$
- Solution:
  - x3 = x8 = x10 = 1, all other xi's are 0
    - Test session 3 includes T1 and T6
    - Test session 8 includes T2 and T5
    - Test session 10 includes T3 and T4
  - Test length = L3 + L8 + L10 = 120
  - Peak power = max {P3, P8, P10} = 3 (Pmax = 4)

A System Example: ASIC Z*



* Y. Zorian, "A Distributed Control Scheme for Complex VLSI Devices," *Proc. VLSI Test Symp.*, April 1993, pp. 4-9.

Test Scheduling for ASIC Z



R. M. Chou, K. K. Saluja and V. D. Agrawal, "Scheduling Tests for VLSI Systems under Power Constraints," *IEEE Trans. VLSI Systems*, vol. 5, no. 2, pp. 175-185, June 1997.

References

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- E. Larsson, *Introduction to Advanced System-on-Chip Test Design and Optimization*, Springer 2005.
- P. Girard, X. Wen and N. A. Touba, “Low-Power Testing,” in System on Chip Test Architectures, L.-T. Wang, C. E. Stroud and N. A. Touba, editors, Morgan-Kaufman, 2008.
- N. Nicolici and P. Girard, Guest Editors, “Special Issue on Low Power Test,” *J. Electronic Testing: Theory and Applications,* vol. 24, no. 4, pp. 325–420, Aug. 2008.