Evaluation of Non-Quasi-Static Effects during SEU in Deep-Submicron MOS Devices and Circuits

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Abstract

In this paper, for the first time, we analyze non-quasi-static (NQS) effects during single-event upsets (SEUs) in deep-submicron (DSM) MOS devices, using extensive 2D device, BSIM4 and Look-Up Table (LUT) simulations. We know that even for DSM transistors and circuits, the quasi-static approximation is valid for most digital applications. However, a single-event particle strike in a memory cell is capable of causing NQS effects which can result in erroneous logic-state prediction. The anomalous effect is attributed to the fast-varying transient (produced during particle-strike), which is able to initiate NQS effects in the transistors of the memory cell. Thus, it becomes important for a circuit designer to incorporate NQS effects during SEU simulation.

1 Introduction

To keep pace with the continuously advancing CMOS technology, it becomes essential to accurately predict circuit performance through simulation. For most digital applications, an efficient simplification is achieved with the quasi-static (QS) approximation, ignoring the finite charging time of the inversion layer charge. However, this approximation causes error in simulation results when the signals are switching very fast, underlining the need for non-quasi-static (NQS) models [1]. These models are reasonably accurate and take into account the carrier transit delay from source to drain. Thus, for analog applications, it is necessary to use NQS models at and near cut-off frequencies, while most digital applications can be still dealt with QS approximation [2].

Single event upsets (SEUs) is an important reliability concern for memories designed for space applications. SEUs are caused when highly energetic particles present in the natural space environment strike sensitive regions of a microelectronic circuit [3]. Depending on various factors, the particle strike may cause no observable effect, a transient disruption of circuit operation, an erroneous logic state termed "upset", or in some cases, even permanent damage to the device or the circuit. Numerical device simulation has been extensively used to provide insight into the response of the devices and small circuits to these particle strikes. Nevertheless, for a circuit designer, SPICE is still of major use for interpreting results and to design for mitigating SEUs. This necessitates modeling of the particle strike, which can be done with some accuracy by injecting a transient current at the struck node in circuit simulation [3].

However, the possible NQS effects that can arise because of the single-event particle strike have not been reported in the literature till date. In this work, we systematically analyze these effects in and around the memory cell during the particle strike. Through extensive device (exact NQS) simulations, Look-Up Table (exact QS) simulations and SPICE/BSIM4 simulations (using QS and NQS models), we have found that the QS approximation does not hold good during SEU and can lead to erroneous logic state prediction of the memory cell.

2 Simulation Methodology

The aim of this paper is to evaluate the difference in the simulation results when QS or NQS models are used while simulating single-event upsets and not to evaluate any particular technology or circuit for SEUs. Thus, a simple yet relevant circuit SRAM in 0.1 μm technology with a resistive load was chosen as the memory cell. Three types of simulations were done to determine the exact QS, exact NQS and modeled QS and NQS behaviour of these devices.

2.1 Device Simulations

2-D device simulations are generally presumed to depict the most accurate behaviour of devices (exact NQS), and

therefore were used as the "ideal" case to compare the other simulations with. Various transistors and the cross-coupled SRAM cell at the device level were designed and simulated using DIOS (process simulator) and DESSIS (device simulator) available in the ISE-TCAD suite [4]. All the transistors were made to conform with the SIA roadmap and had transit times comparable to standard devices.

2.2 LUT Simulations

The second set of simulations were done using the Look-Up Table (LUT) approach. LUT approach has recently attracted much attention primarily because of the problems in accurate modeling of advanced and novel devices [5]. For this work, we have utilized the LUT methodology implemented in SEQUEL [6], a general-purpose public-domain circuit simulator developed at IIT Bombay. Here, a table of DC (QS) terminal currents and charges is first generated using ISE-2D device simulations. A suitable interpolation scheme is then employed to obtain the values of I and Q at any arbitrary point, thus making the LUT approach as the exact QS model [7]. As we are not making any approximations in extracting the terminal charges and currents of the MOS device. To validate this point, we have simulated an NMOS inverter with resistive load of 100 kΩ. Fig. 1 shows the simulation results obtained from 2D-device simulations, LUT and BSIM4 simulations for a pulse input. The results show an exact match between the LUT and 2D device simulations.

2.3 BSIM4 QS and NQS Simulations

A third set of simulations is then done using SPICE QS and NQS models with the extracted BSIM4 parameters for the 0.1 μm device, using ISExtract available in ISE-TCAD suite. A rigorous parameter extraction routine is followed to ensure a proper match between the BSIM4 results and the device simulations. Fig. 2 shows the matching of the modeled capacitances with the actual capacitances obtained from device simulations. From Fig. 1, we can notice that the results obtained by using extracted BSIM4 parameters matches well with that of 2D device simulations.

To model the electrical response of the single-event particle strike, a time-dependent current source is used [8]. Traditionally a double-exponential current source is used for this purpose. However, the inaccuracy of this model has been noted in the literature [3]. Therefore to avoid any errors in the modeling of current source, we have used the transient current extracted from the actual SEU simulation on a discrete device biased at the same initial conditions as the NMOS transistor of the SRAM. This takes into account various charge enhancement effects because of SEU and therefore is the most accurate, except for the fact that

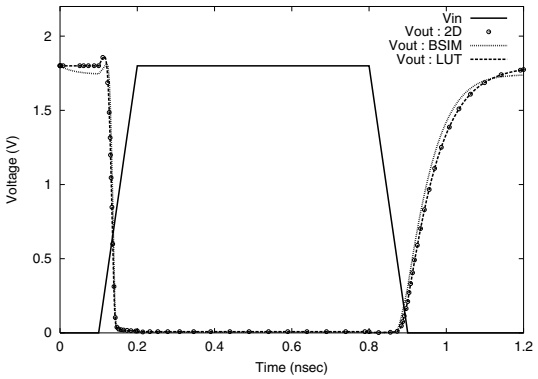

Figure 1. Simulation results of NMOS inverter with resistive load of 100 kΩ obtained from 2D device simulations, LUT simulations, and BSIM4 QS model; Vdd=1.8 V.

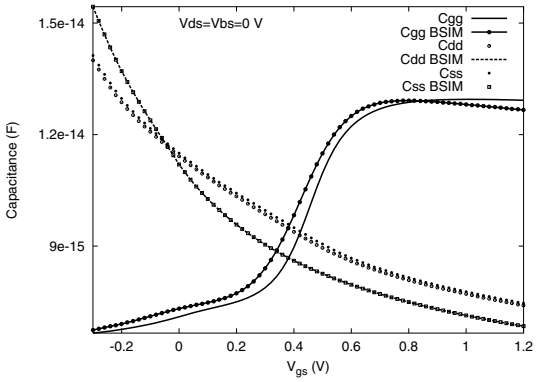

Figure 2. Comparison of BSIM4 extracted capacitances with device simulations.

entire SEU simulation is done at constant bias. This transient current (I_{SEU}), is then injected into the above three simulation setups.

In the actual SEU simulation on the discrete device, the length of the heavy ion track was made 0.5 μm. The radiation charge was Gaussian in space and time, with a characteristic radius of 0.5 μm and a characteristic time of 2 ps. The metric to define particle energy is LET (linear energy transfer), which describes the energy lost per unit track length, as the particle passes through the device. In our results LET would be quoted with the units of pC/μm, which refers to the amount of charge the particle has deposited per micron of the track. The discrete device was biased in the OFF state (V_{GS} = 0, V_{DS} = V_{DD} = 1.8 V) and the particle hit is done at the drain-gate edge.

3 NQS Effects in SRAM Cell

For every simulation that was done, an SEU device simulation was performed on a discrete device at the same bias to extract the transient drain current (I_{SEU}). This current was then injected into the simulation setups (as shown in Fig. 3). The nomenclature for various simulations is as follows. "QS" and "NQS" refer to BSIM4 QS and BSIM4 NQS simulations with injected current to model SEU. "Device" refers to the 2D-device simulation with injected current. "LUT" refers to the LUT simulation with injected current.

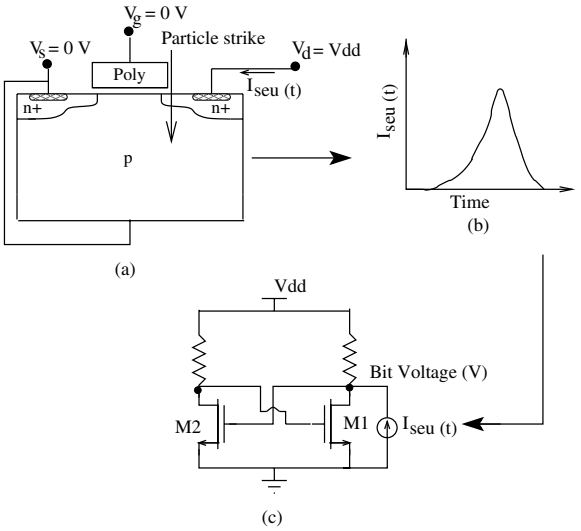

Figure 3. Schematic of the SEU current generation and its incorporation in circuit simulation.

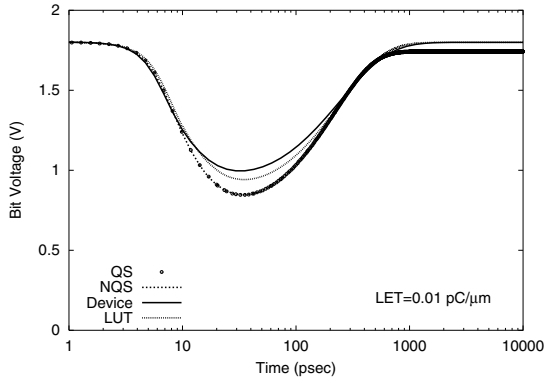

Figure 4. Comparison of various simulations at LET of 0.01 pC/μm.

Fig. 4 shows the simulation response of the SRAM when injected with a transient current resulting from a particle strike of relatively low energy (0.01 pC/μm). It is evident that there exists only a marginal difference between device and LUT simulations, whereas the BSIM4 QS and NQS simulations (almost identical to each other), are further away from the device simulation results. As the particle energy is increased, the magnitude of resulting transient also increases. The results of particle-strike with energy of 0.016 pC/μm are given in Fig. 5. At this energy, the discrepancy arises between the BSIM4 QS and NQS and results in the prediction of flipping with QS model. However, the NQS model still shows recovery, as does LUT and device simulations.

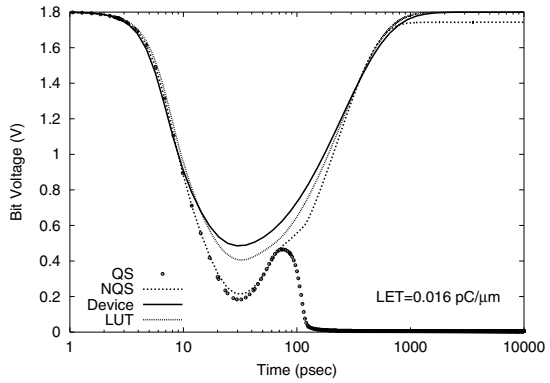

Figure 5. Comparison of various simulations at LET of 0.016 pC/μm.

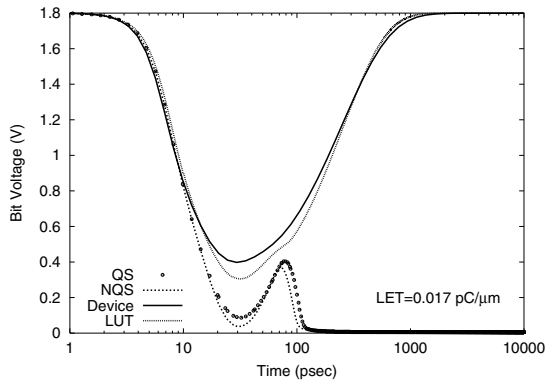

Figure 6. Comparison of various simulations at LET of 0.017 pC/μm.

At higher particle energy (0.017 pC/μm), BSIM4 NQS simulation also shows flipping, unlike the LUT and device simulations (Fig. 6). This result, however, is not sufficient to make inferences with regards to relative accuracies of BSIM4, LUT and device simulations. At still higher energy, we observe a flip in LUT simulation (see Fig. 7),

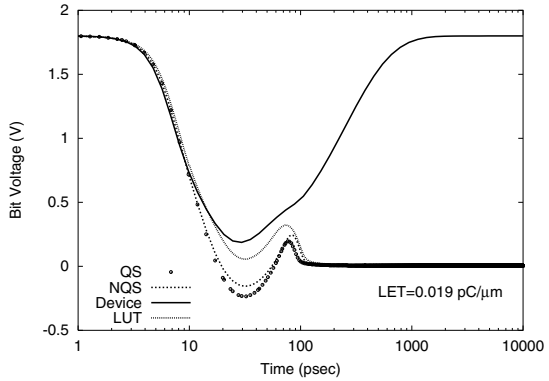

Figure 7. Comparison of various simulations at LET of 0.019 pC/μm.

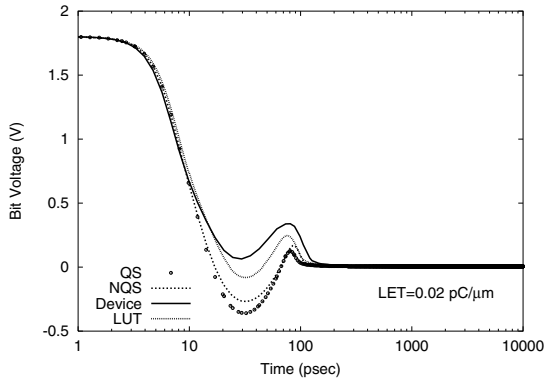

Figure 8. Comparison of various simulations at LET of 0.02 pC/μm.

even though device simulations recover. The difference in logic-state predictions by LUT (exact QS) and device (exact NQS) and BSIM4 QS and NQS simulations clearly underlines the presence of NQS effects during SEU. It can be noted that device simulations (exact NQS) flips at an energy of 0.02 pC/μm, which is highest among all the injected current simulations (Fig. 8). The results are summarized in Table 1. This fact and the delayed flipping of BSIM4 NQS results (in comparison with BSIM4 QS) suggests that NQS effects slow-down the upset process. This is discussed in the following sub-section.

3.1 Discussion

The upset process in SRAMs is strongly dependent on the active feedback in the cross-coupled inverter pair. Because of the single event particle strike at a sensitive location in the SRAM (typically the drain of the OFF NMOS transistor), charge collected at the junction results in a current transient. The transient current flows through the resistor and causes a voltage drop at the drain of NMOS. This voltage transient is actually fed as input to the cross-coupled inverter and if the voltage drop exceeds a threshold, a wrong logic state is triggered and upset occurs [9]. However, during the particle-strike, the voltage changes so rapidly that it is unreasonable to assume that the NMOS transistor of the feedback inverter would be able to respond in a quasi-static manner. However, the quasi-static simulations would still assume instantaneous response from the transistor M2 (see Fig.3). Hence, if the voltage transient falls below the threshold of M2, an upset would occur.

Table 1. Comparison of critical LETs for various simulations

Simulation Type	Critical LET (pC/μm)
BSIM4 QS	0.016
BSIM4 NQS	0.017
LUT (Exact QS)	0.019
2-D Device (Exact NQS)	0.02

This, however, does not happen. The feedback transistor (M2) is only able to produce a delayed (non-quasi-static) response to such a fast varying transient, thus helping the cell to recover at an energy at which QS simulations *just* predicts a flip, as seen in the last sub-section.

The subsequent step to realizing the importance of NQS effects during SEU was to understand why QS approximation results in early prediction of flipping. This was understood with the help of four simulation setups, in which each of the transistor model was either QS or NQS. The simulation result for these setups for particle-strike with energy of 0.016 pc/μm are given in Fig. 9. As can be seen from

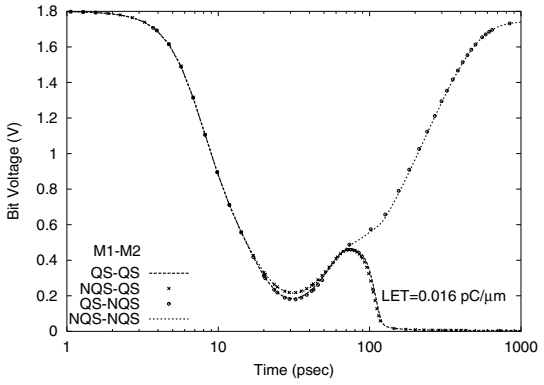

Figure 9. Comparison of BSIM4 simulations at LET of 0.016 pC/μm

the figure, at this energy, complete QS simulation predicts a flip. It can also be seen that no substantial difference appears when NQS model is used only for the struck transistor. However, the other two simulations, complete NQS and the one in which the feedback transistor is modeled non-quasi-statically recover. At a slightly higher energy (0.0164 pC/μm), even the simulation with NQS model for feedback transistor flips. This underlines the fact that NQS effects occurring in the feedback transistor are more important to SEU as compared to those happening in the struck transistor itself. It was found that the complete NQS simulation flips at the highest energy among all : 0.017 pC/μm. The above results are tabulated in Table 2. It brings out the fact that since the QS approximation assumes instantaneous response from the feedback transistor, it results in the prediction of an early and erroneous flipping.

Table 2. Comparison of critical LETs for various BSIM4 Simulations

Model Type (M1-M2)	Critical LET (pC/μm)
QS-QS	0.016
NQS-QS	0.016
QS-NQS	0.0164
NQS-NQS	0.017

3.2 Limitation of QS Model

It is a general belief (and a rule of thumb), that QS models hold true till the rise-time (t_r) and fall-time (t_f) of the switching signal are greater than 20 times the transit time (τ_{tr}) of the device [1], [10]. This has been verified experimentally before, and also through our simulation results presented in this section. Transit time of the device can be defined as the time that carriers take to move from source to drain. For our calculation, we have integrated the velocity of the carriers in the inversion layer from the source to the drain. The transit time for the device in use was 0.8 ps. It is well known that onset of NQS effects causes an unrealistically large drain current spike during fast turn-on. Thus the next step was to simulate such fast turn-ons for different rise-times, first with exact NQS model (device simulations) and then, with exact QS (LUT). NQS current components were then extracted as the difference between the currents calculated by device simulation and those by LUT simulations. Fig. 10 shows the drain NQS current component for different rise times of the gate transient, keeping drain voltage at 1.8 V. As the rise time of the input signal goes high, the magnitude of the drain NQS current component diminishes. The results are quantified in Table 3. The first column indicates the rise time of the input signal, the second column

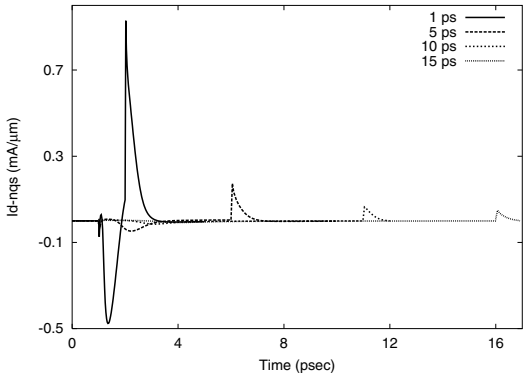

Figure 10. Drain NQS current component; the difference between drain current obtained from 2D device simulations and LUT simulations for different rise times of the gate voltage.

shows the maximum value of the drain NQS current component when the gate voltage is rising, and the third column shows the ratio of drain NQS current component to the actual drain current obtained from 2D device simulations. As can be seen, NQS currents are negligible for t_r of 20 ps, though, they start becoming prominent as t_r is decreased.

Table 3. Comparison of NQS current components as a function of rise-time

t_r (psec)	$I_{dNQSmax}$ (μA)	I_{dNQS}/I_d (%)
20	6.6	14
15	7.9	37
10	15.1	42.12
5	47.5	63
1	475	115

It is important to note here that origin of such fast varying transients, which may cause substantial NQS effects, is very uncommon. As the technology scales, both t_r and τ_{tr} are scaled and thus, the relationship ($t_r > 20\tau_{tr}$) is still maintained, and hence, for simulating most digital circuits, the QS model is still valid. Looking at the SRAM problem in this context, we find that fall time of any SEU-induced voltage transient is well within the range ($t_r < 20\tau_{tr}$), making it possible for NQS effects to occur, not only in transistors of the memory cell, but also in other transistors.

4 Conclusion

In this paper, we have systematically analyzed NQS effects that can occur during SEU in SRAM cell, which was designed for deep-submicron CMOS technology. The SEU-induced current was extracted directly from device simulations on a discrete device to avoid any inaccuracies in its modeling. We have also used LUT based simulations for a close matching with device simulations, since LUT approach does not require any modeling for the devices. Thus, four types of simulation scheme were resorted to: exact NQS (device simulation), exact QS (LUT simulations) and modeled QS and NQS (BSIM4).

We note that SEU in a deep-submicron CMOS SRAM cell is able to initiate fast falling transients which can cause significant NQS effects. These effects result in erroneous calculation of logic state after SEU if appropriate NQS models are not used, and thus can have serious impact on SEU reliability assessment of any given circuit.

Acknowledgment

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